EE 330
Lecture 37

Digital Circuits

Characterization of CMOS Inverter
Static CMOS Logic Gates

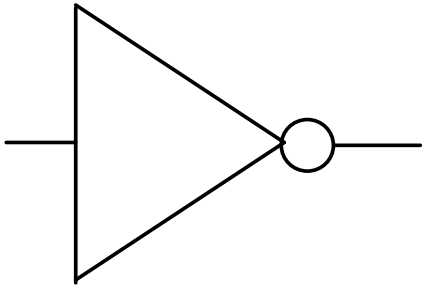
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

Review from last time:

The basic logic gates

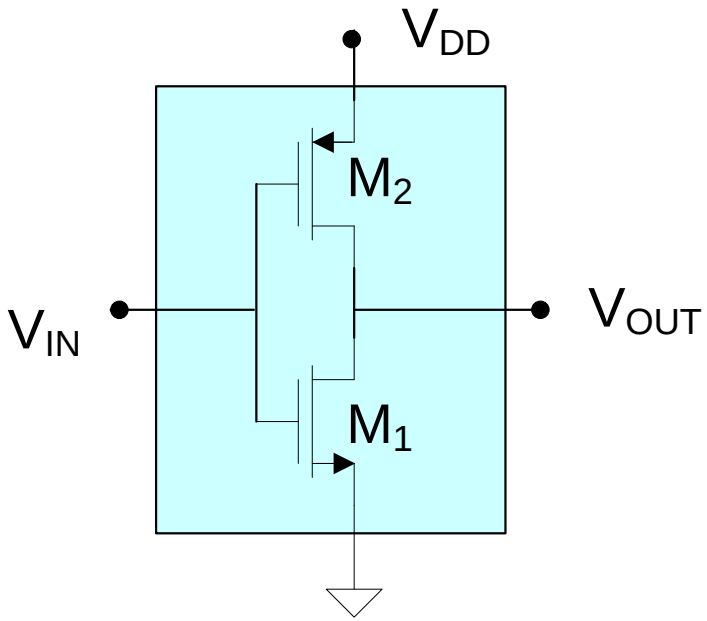
It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.

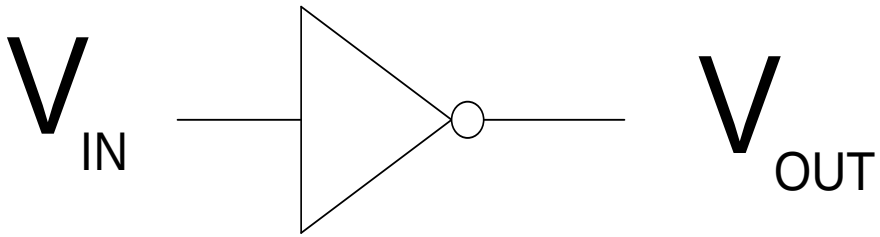


What characteristics are required and desirable for an inverter to form the basis for a useful logic family?

Review from last time:

Transfer characteristics of the static CMOS inverter





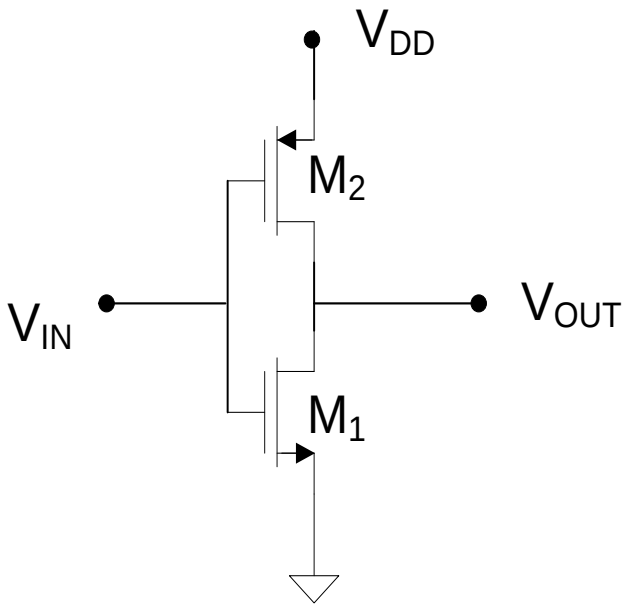
Review from last time:

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

$$V_{IN} = \frac{V_{Tn}\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}} + V_{DD}+V_{Tp}\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}{\sqrt{\frac{\mu_n C_{OXn}}{2}\frac{W_1}{L_1}}+\sqrt{\frac{\mu_p C_{OXp}}{2}\frac{W_2}{L_2}}}$$



Since $C_{OXn} \cong C_{OXp} = C_{OX}$ this can be simplified to:

$$V_{IN} = \frac{V_{Tn}\sqrt{\frac{W_1}{L_1}} + V_{DD}+V_{Tp}\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}{\sqrt{\frac{W_1}{L_1}}+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{L_2}}}$$

valid for:

$V_{GS1} \geq V_{Tn}$ $\quad V_{DS1} \geq V_{GS1} - V_{Tn}$ $\quad V_{GS2} \leq V_{Tp}$ $\quad V_{DS2} \leq V_{GS2} - V_{T2}$

thus, valid for:

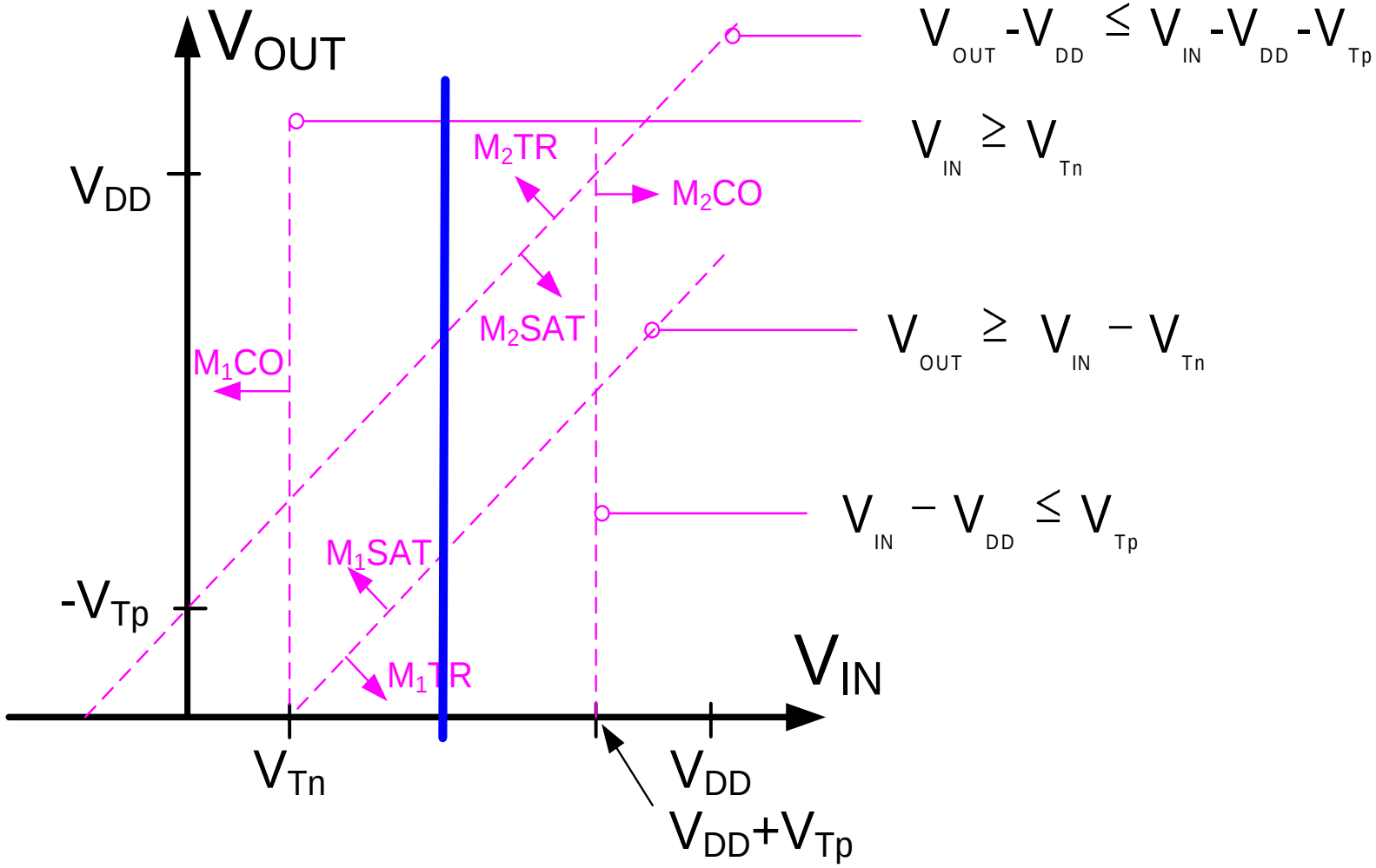
$V_{IN} \geq V_{Tn}$ $\quad V_{OUT} \geq V_{IN} - V_{Tn}$ $\quad V_{IN} - V_{DD} \leq V_{Tp}$ $\quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$

Review from last time:

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

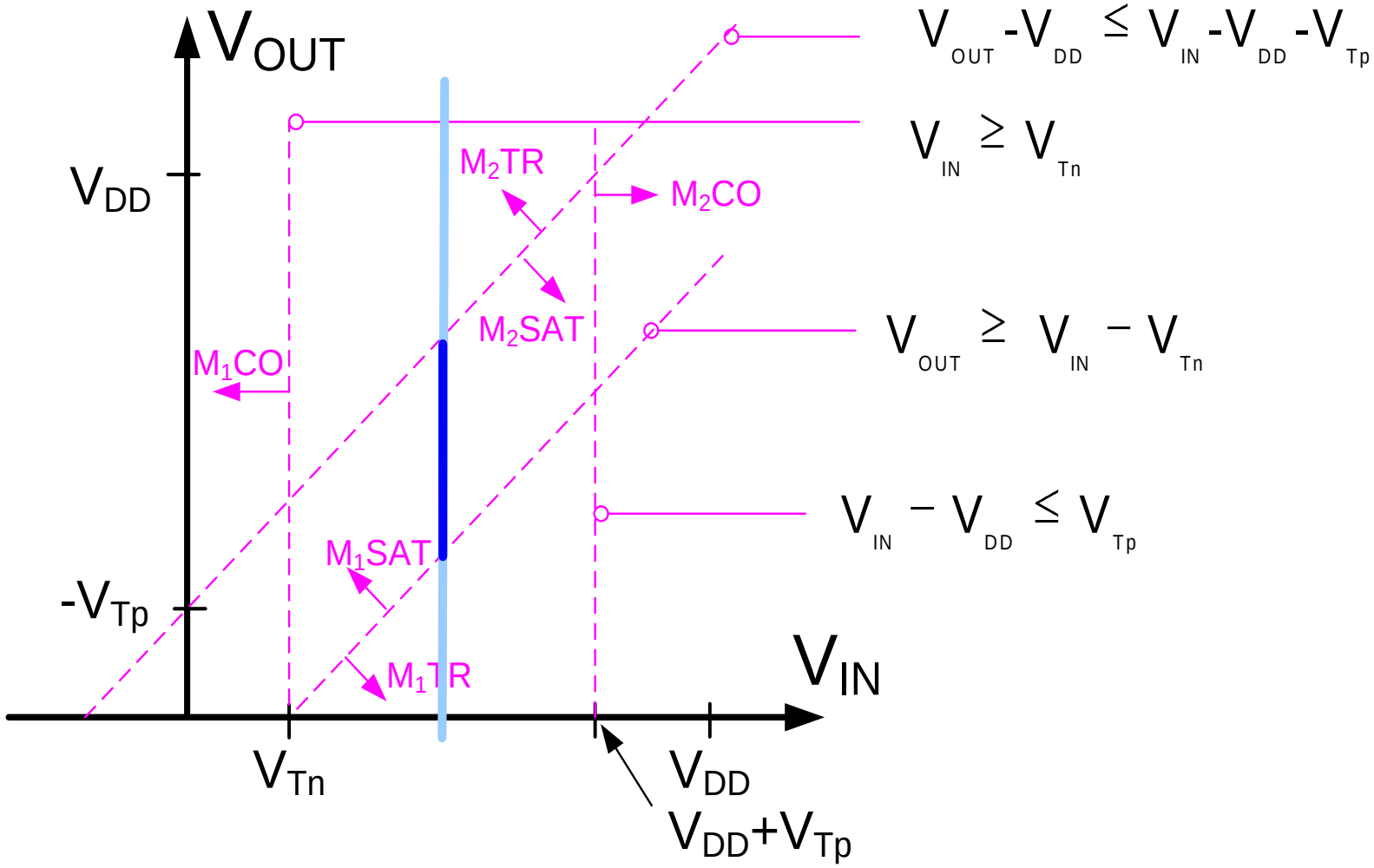


Review from last time:

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 3 M_1 sat, M_2 sat

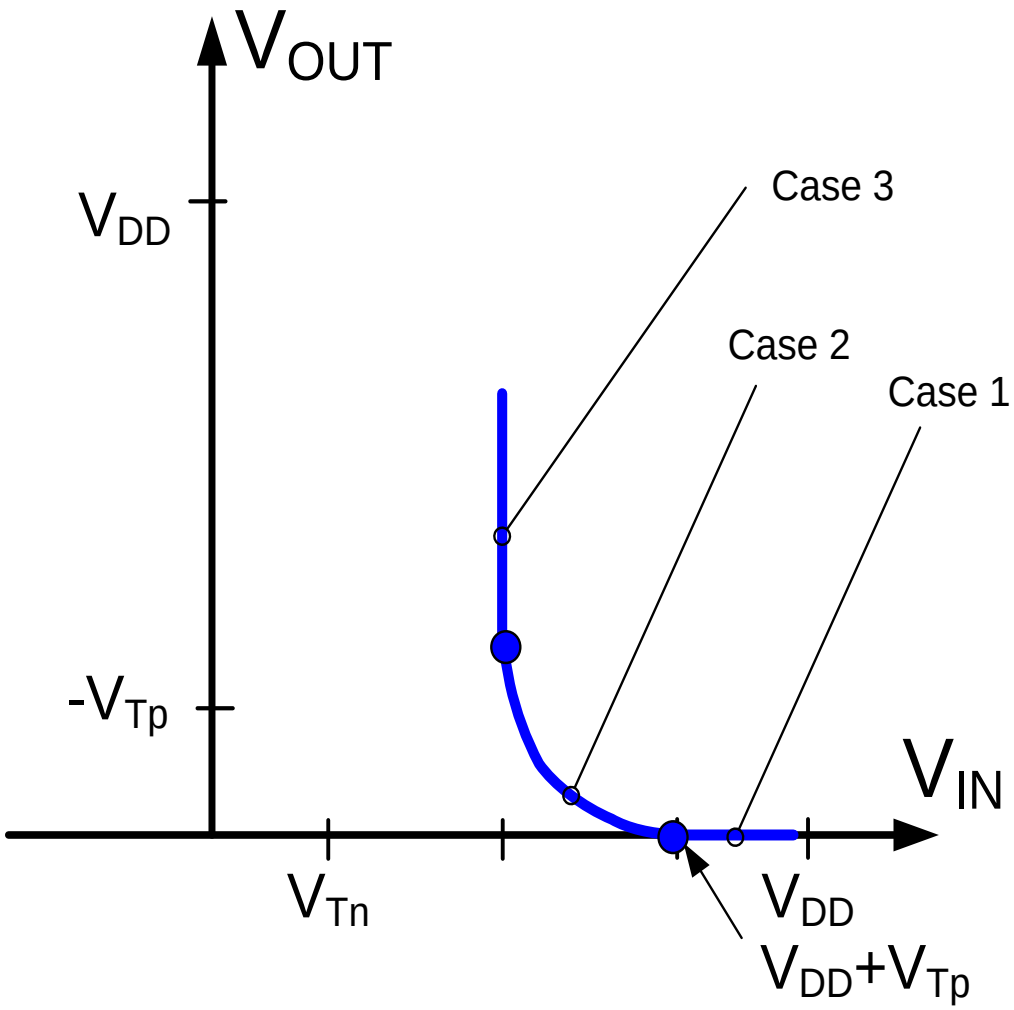


Review from last time:

Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

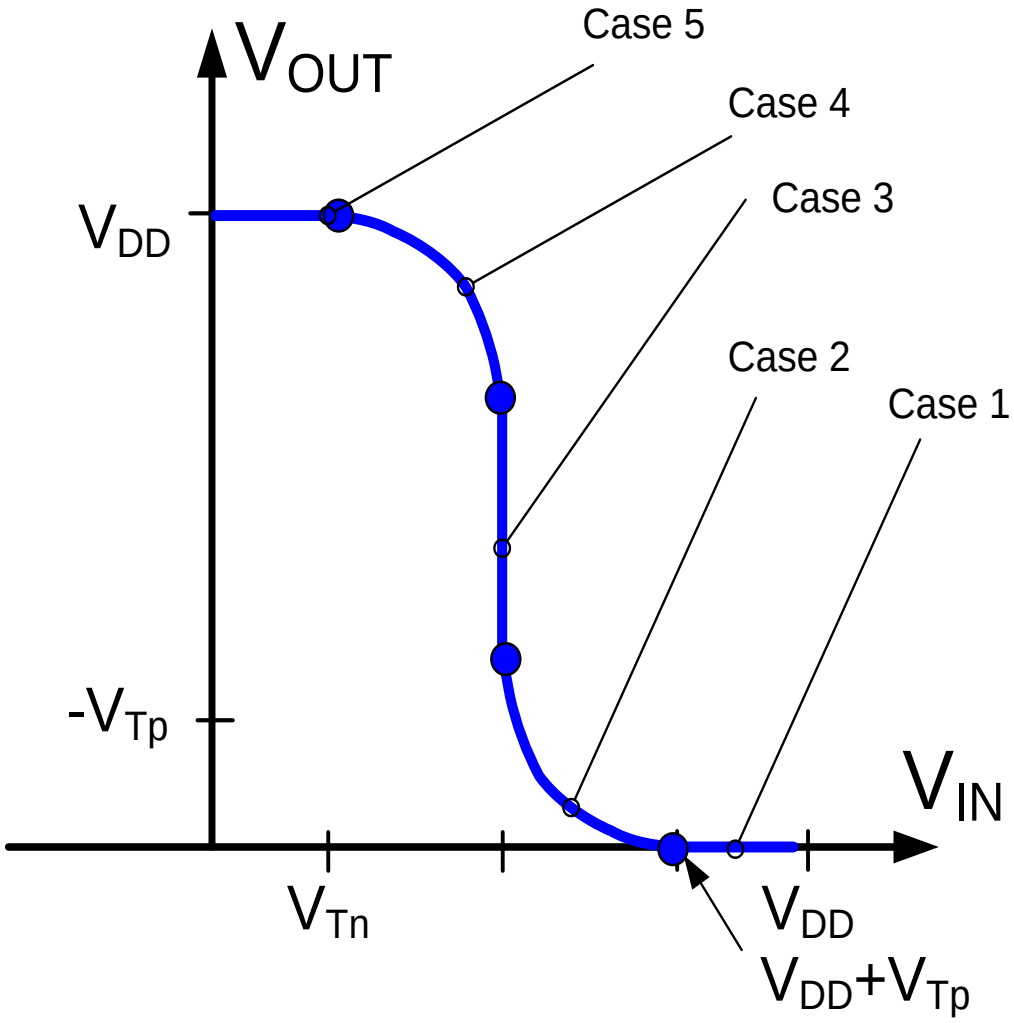
Partial solution:



Review from last time:

Transfer characteristics of the static CMOS inverter

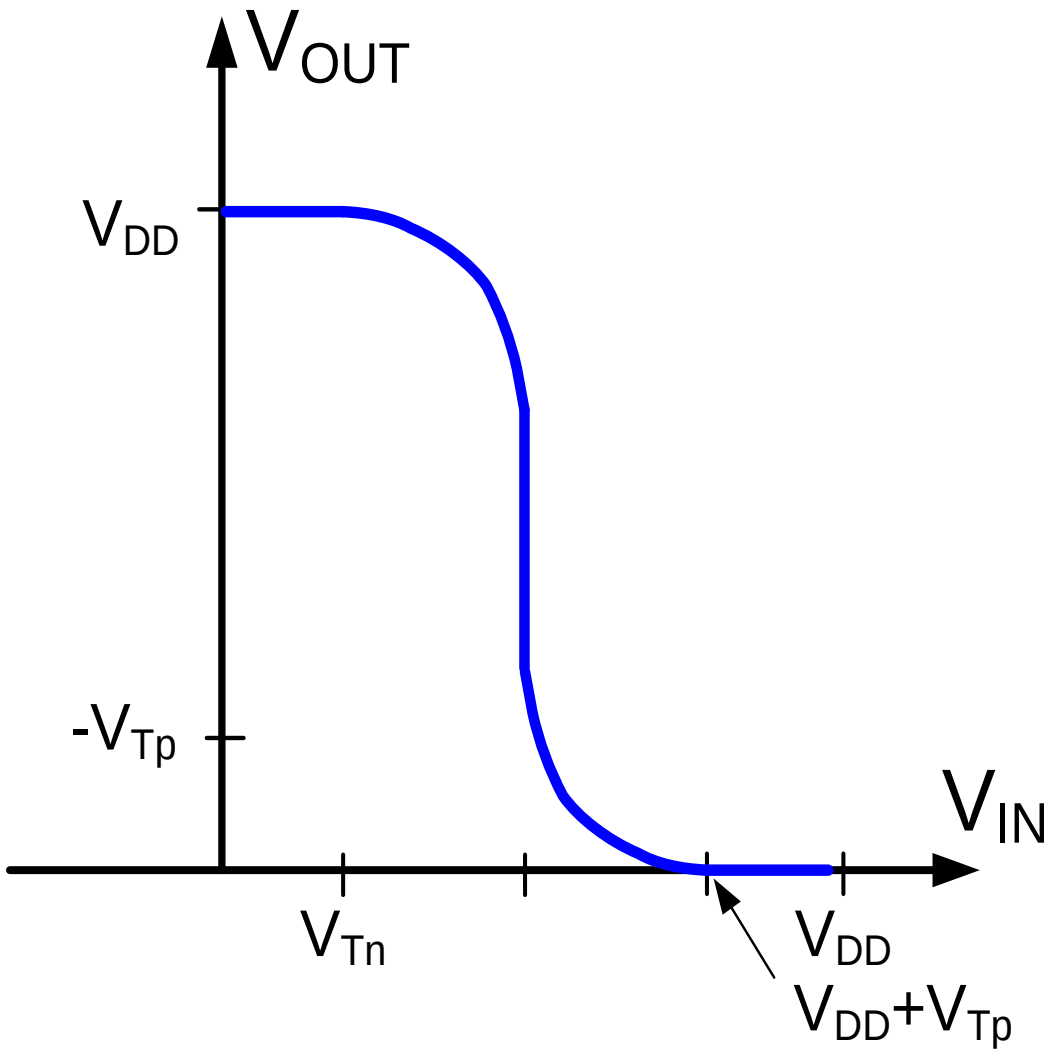
(Neglect λ effects)



Review from last time:

Transfer characteristics of the static CMOS inverter

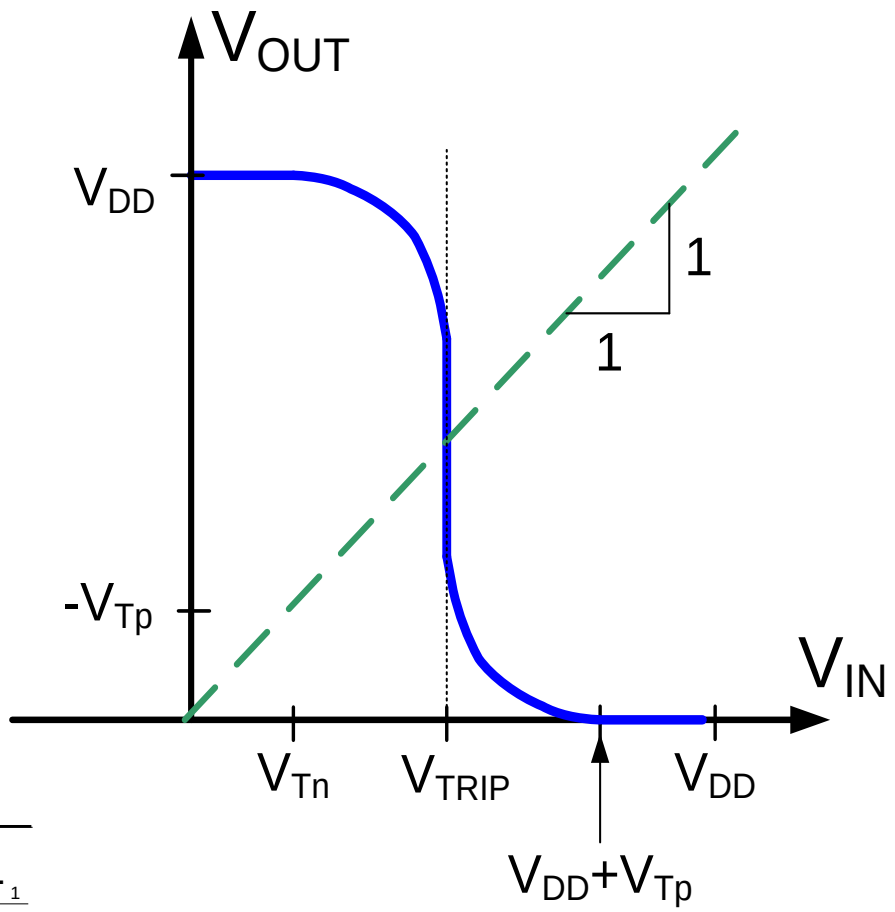
(Neglect λ effects)



Review from last time:

Transfer characteristics of the static CMOS inverter

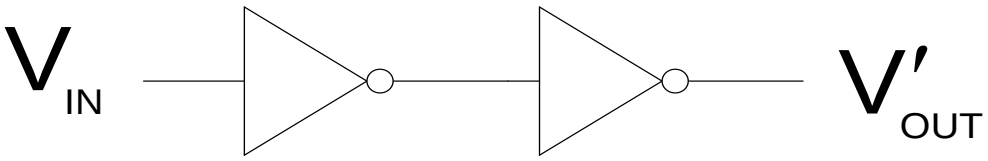
(Neglect λ effects)



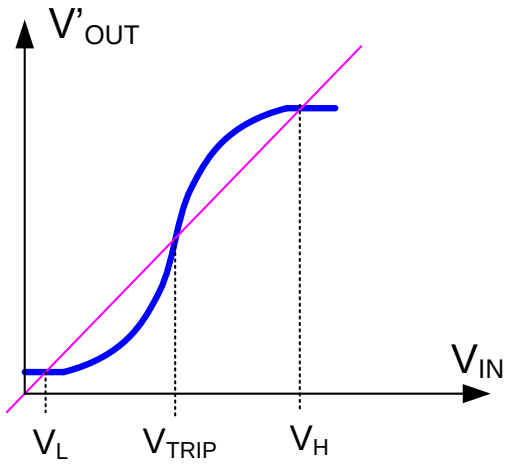
From Case 3 analysis:

$$V_{IN} = \frac{V_{Tn} + V_{DD} + V_{Tp}\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

Inverter Transfer Characteristics of Inverter Pair

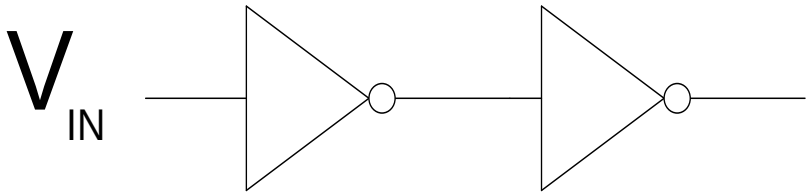


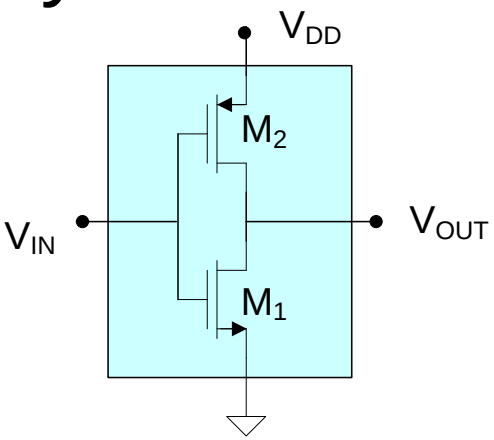
What are V_H and V_L?

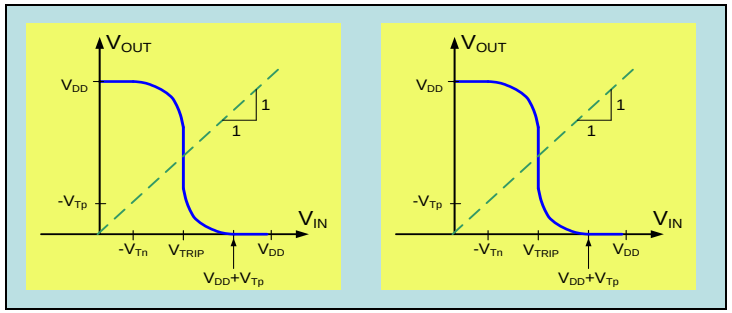


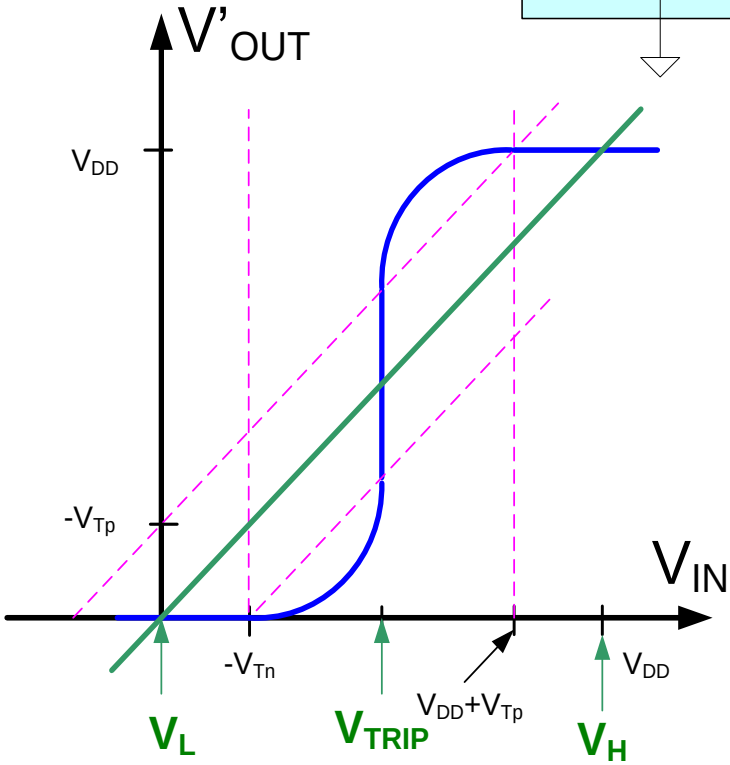
Find the points on the inverter pair transfer characteristics where V_{OUT}'=V_{IN} and the slope is less than 1

Inverter Transfer Characteristics of Inverter Pair for THIS Logic Family





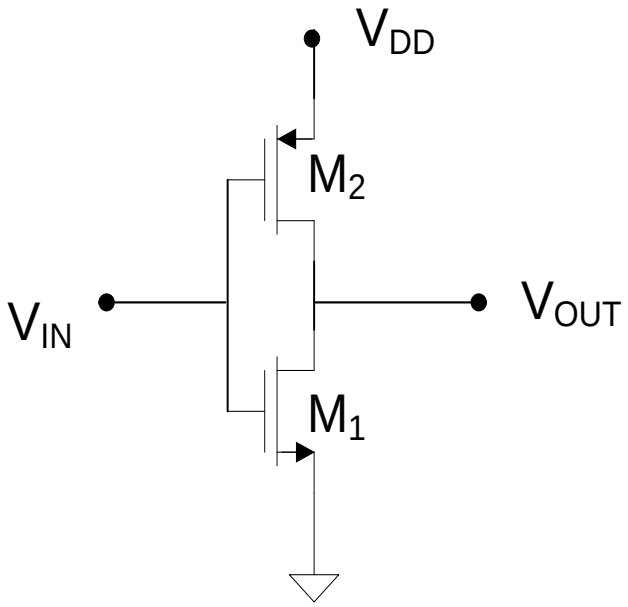




$V_H = V_{DD}$ and $V_L = 0$

Note this is independent of device sizing for THIS logic family !!

Sizing of the Basic CMOS Inverter

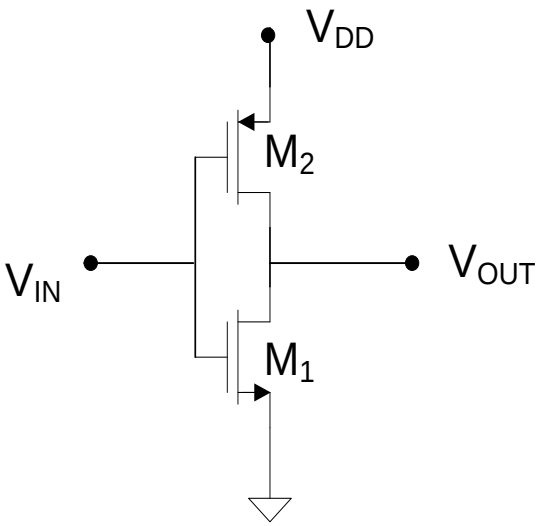


The characteristic that device sizes do not need to be used to establish V_H and V_L logic levels is a major advantage of this type of logic

How should M_1 and M_2 be sized?

How many degrees of freedom are there in the design of the inverter?

How should M_1 and M_2 be sized?



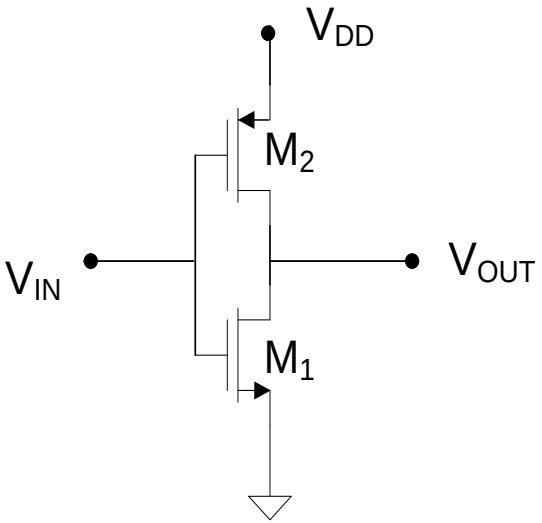
How many degrees of freedom are there in the design of the inverter?

$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom

But in basic device model and in <u>most</u> performance metrics, W_1/L_1 and W_2/L_2 appear as ratios

$\{ W_1/L_1, W_2/L_2 \}$ effectively 2 degrees of freedom

How should M_1 and M_2 be sized?



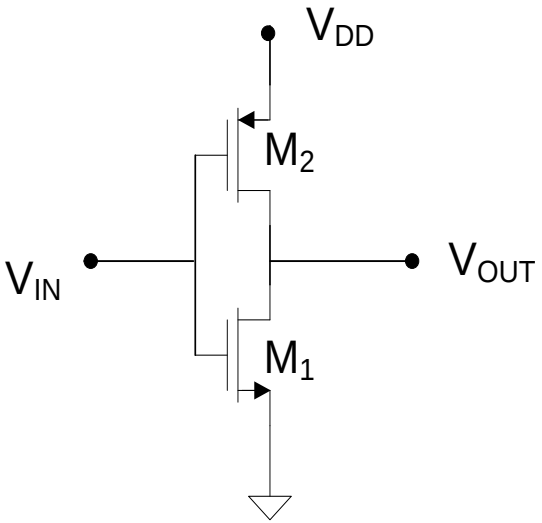
$\{ W_1, W_2, L_1, L_2 \}$ 4 degrees of freedom Usually pick $L_1 = L_2 = L_{min}$

$\{ W_1/L_1, W_2/L_2 \}$ effectively 2 degrees of freedom

How are W_1 and W_2 chosen?

Depends upon what performance parameters are most important for a given application!

How should M_1 and M_2 be sized?



Usually pick $L_1=L_2=L_{min}$

$\{ W_1/L_1, W_2/L_2 \}$ 2 remaining degrees of freedom

One popular sizing strategy:

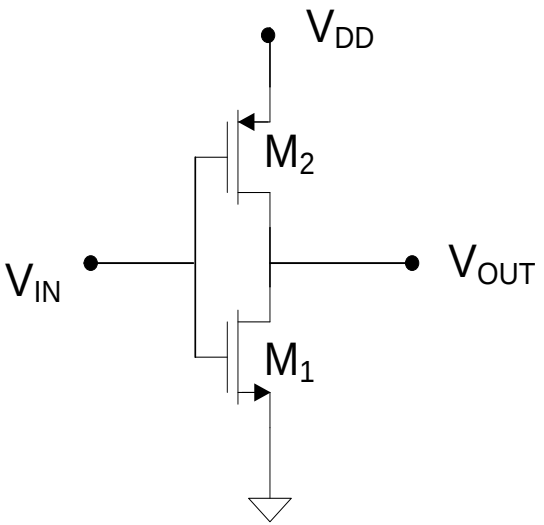
1. Pick $W_1=W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$

How should M_1 and M_2 be sized?

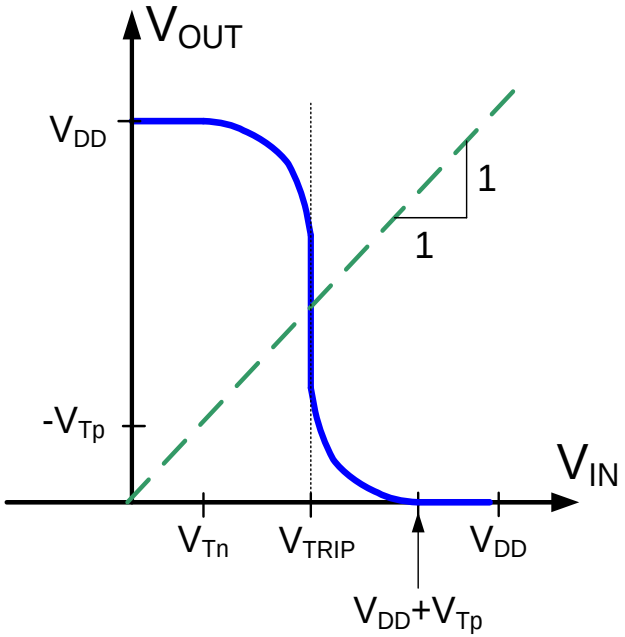
pick $L_1=L_2=L_{min}$

One popular sizing strategy:

1. Pick $W_1=W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$



Observe Case 3 provides expression for V_{TRIP}



Thus, at the trip point,

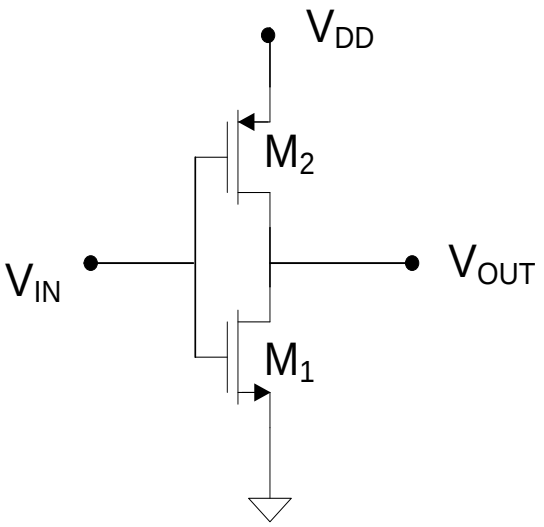
$$V_{OUT}=V_{IN}=V_{TRIP}=\frac{V_{Tn}+V_{DD}+V_{Tp}\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

How should M_1 and M_2 be sized?

pick $L_1=L_2=L_{min}$

One popular sizing strategy:

1. Pick $W_1=W_{MIN}$ to minimize area of M_1
2. Pick W_2 to set trip-point at $V_{DD}/2$



Typically $V_{Tn}=0.2V_{DD}$, $|V_{Tp}|=0.2V_{DD}$

$$V_{TRIP} = \frac{V_{Tn} + V_{DD} + V_{Tp}\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}\frac{L_1}{L_2}}}$$

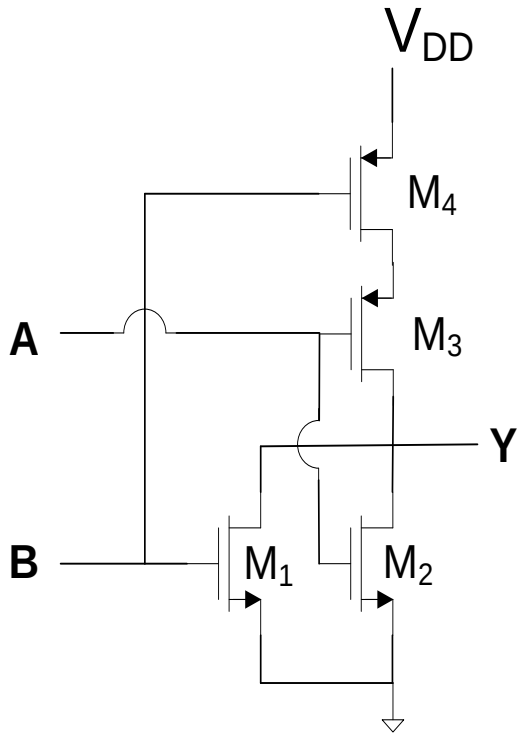
$$\therefore \quad \frac{V_{DD}}{2} = \frac{0.2V_{DD} + V_{DD} - 0.2V_{DD}\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}{1+\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2}{W_1}}}$$

Solving this equation for W_2, obtain

$$W_2 = W_1\left(\frac{\mu_n}{\mu_p}\right)$$

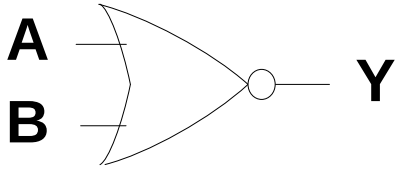
Other sizing strategies are used as well and will be discussed later !

Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

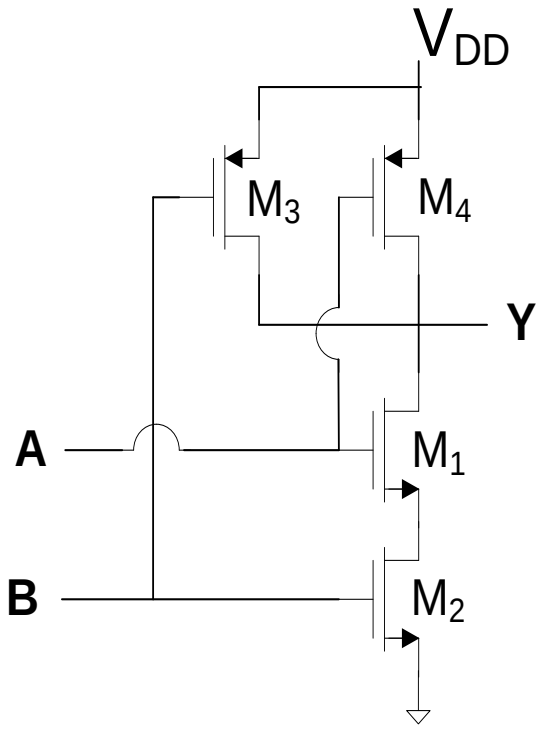
Truth Table



Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate

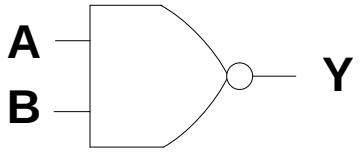
Extension of Basic CMOS Inverter to Multiple-Input Gates



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

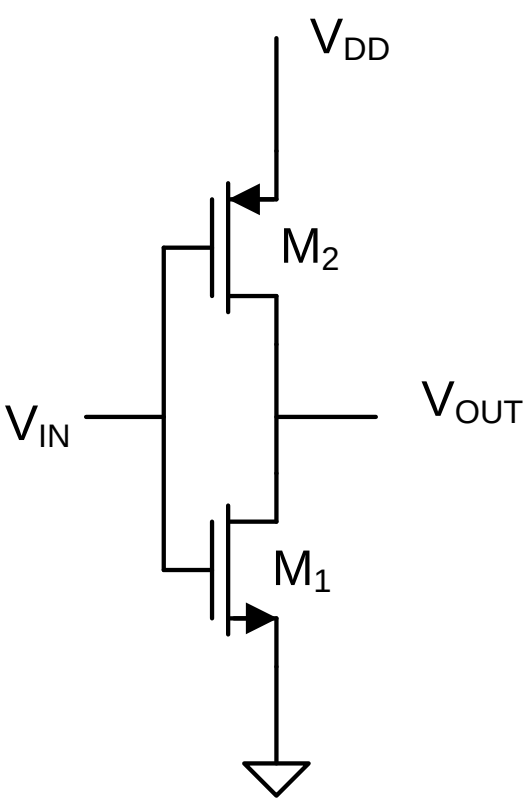
Truth Table

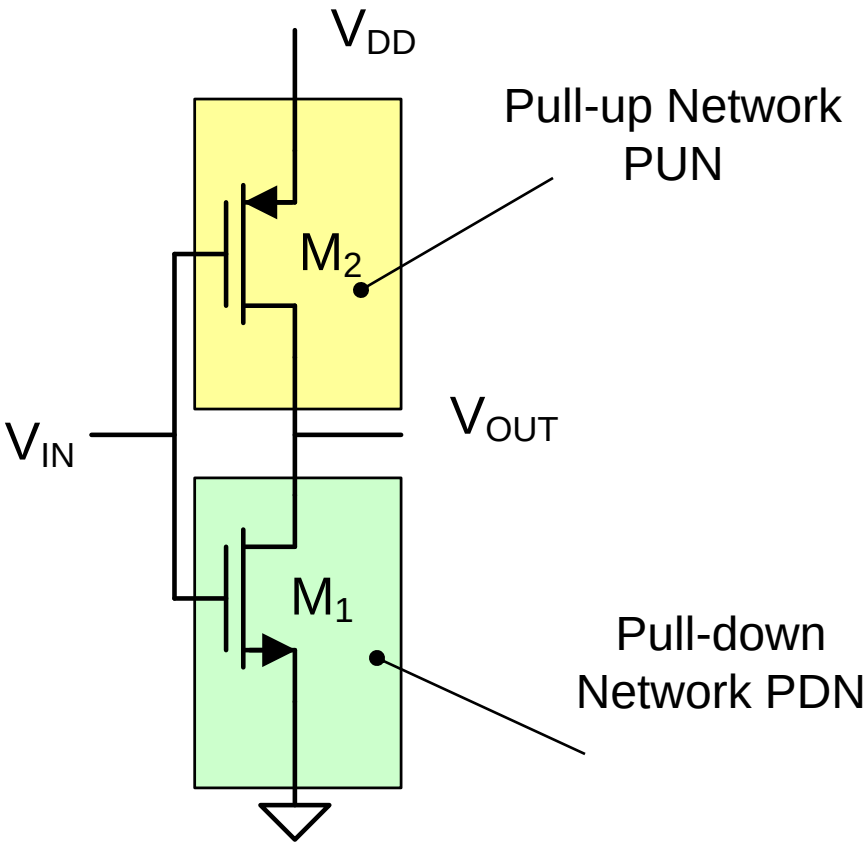
Performs as a 2-input NAND Gate



Can be easily extended to an n-input NAND Gate

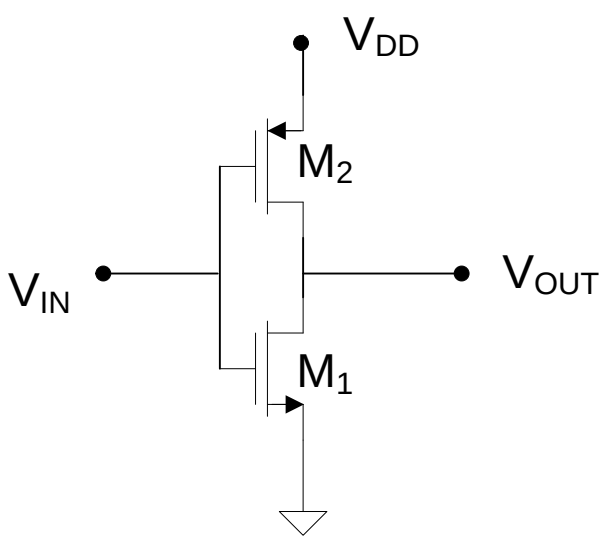
Static CMOS Logic Family

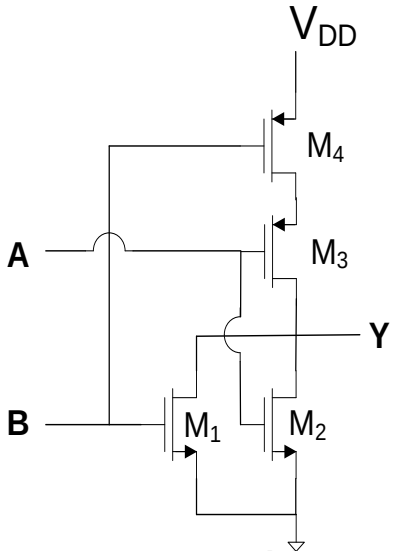


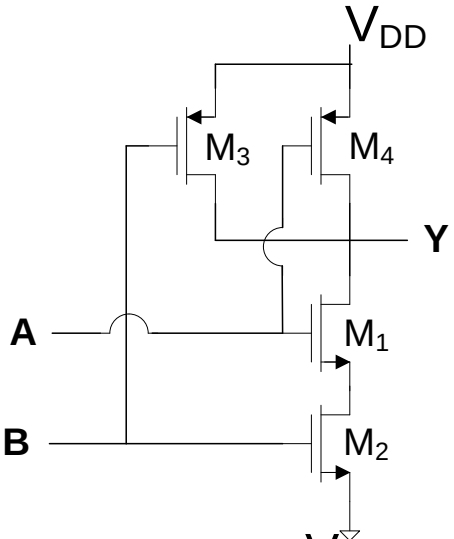


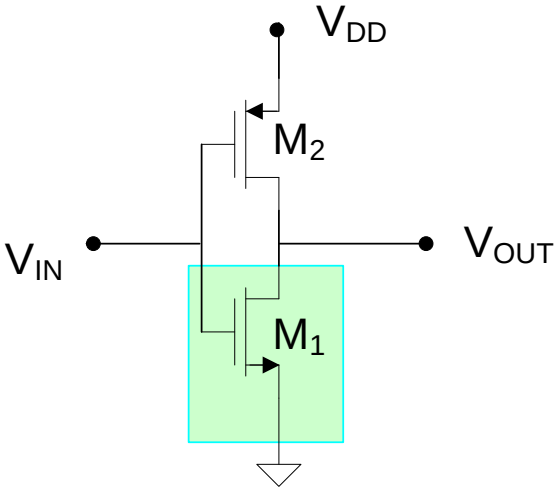
Observe PUN is p-channel, PDN is n-channel

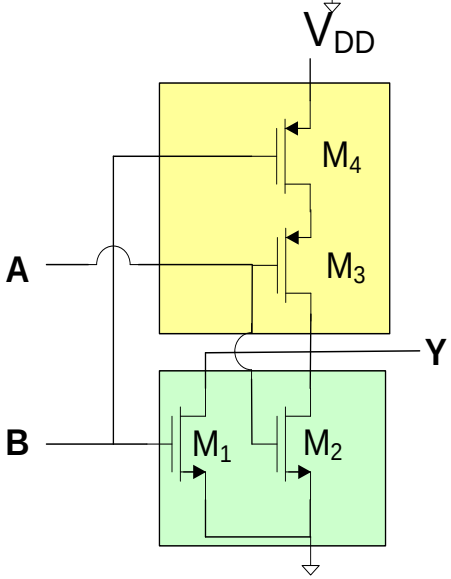
Static CMOS Logic Family

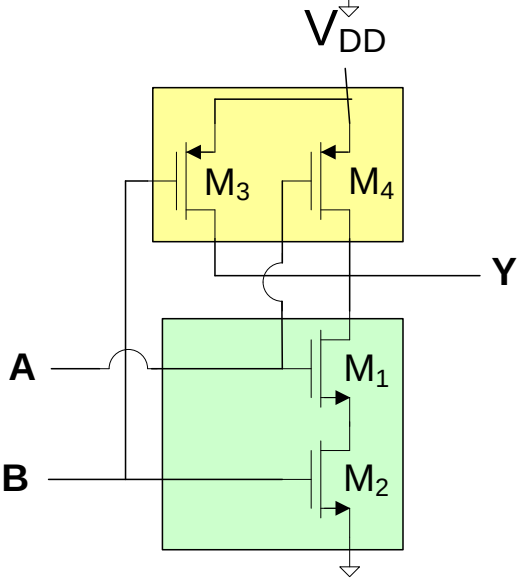






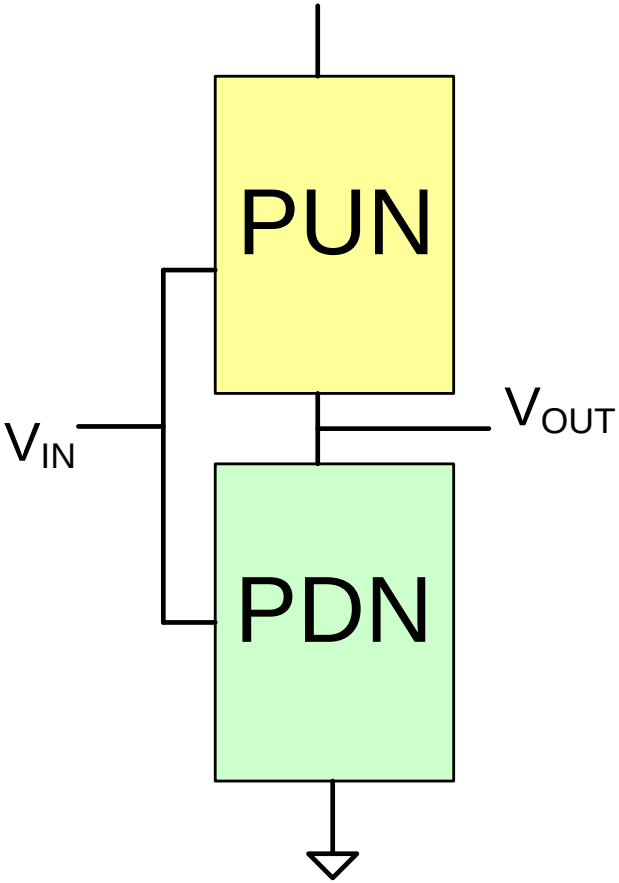




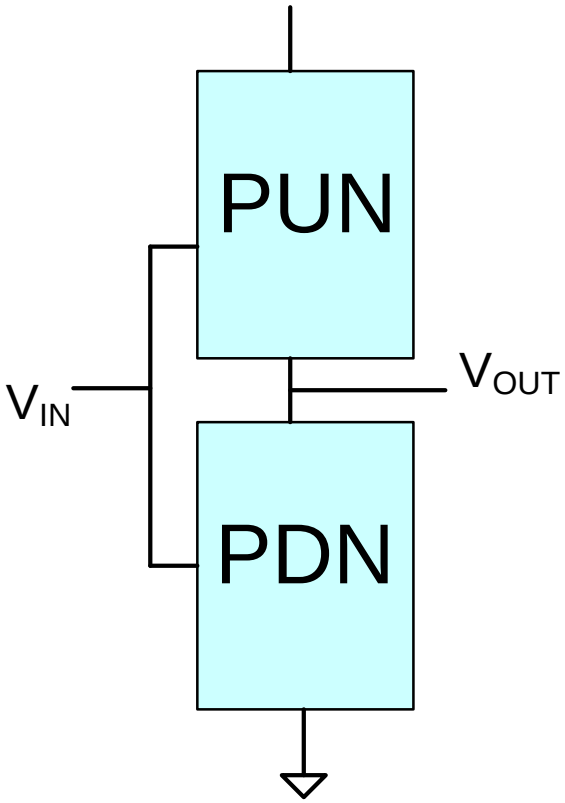


n-channel PDN and p-channel PUN

General Logic Family

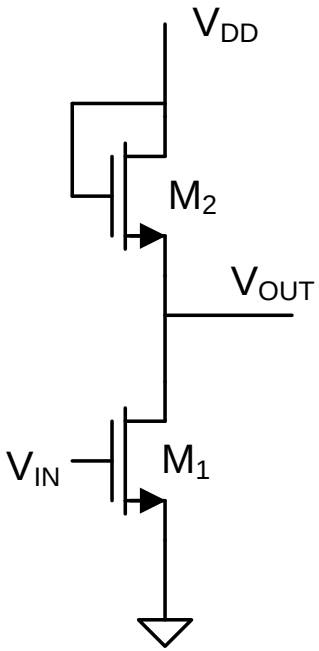


p-channel PUN
n-channel PDN

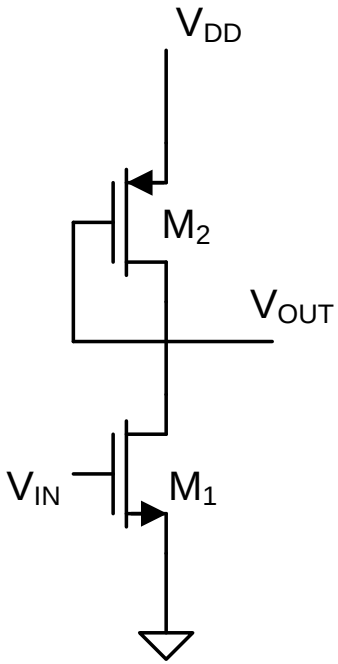


Arbitrary PUN
and PDN

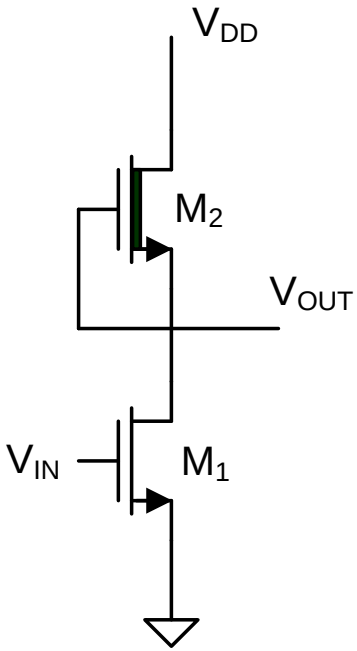
Other CMOS Logic Families



Enhancement
Load NMOS

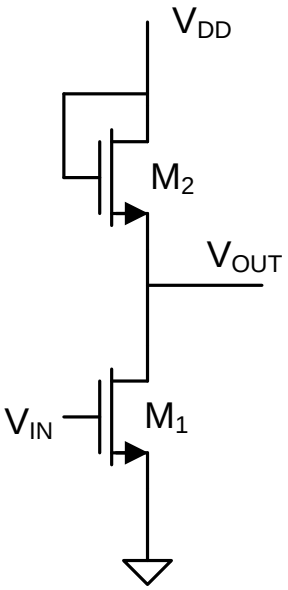


Enhancement Load
Pseudo-NMOS

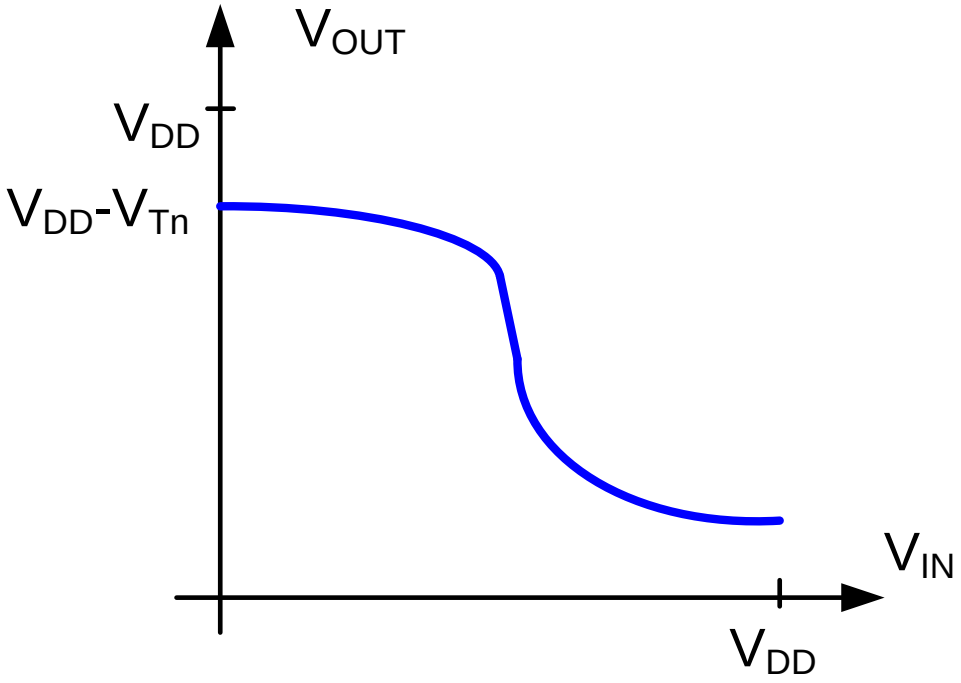


Depletion
Load NMOS

Other CMOS Logic Families

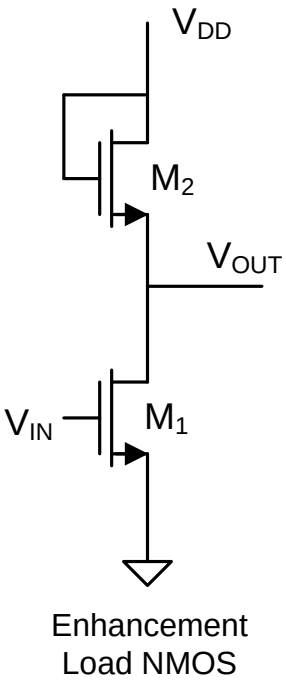


Enhancement
Load NMOS

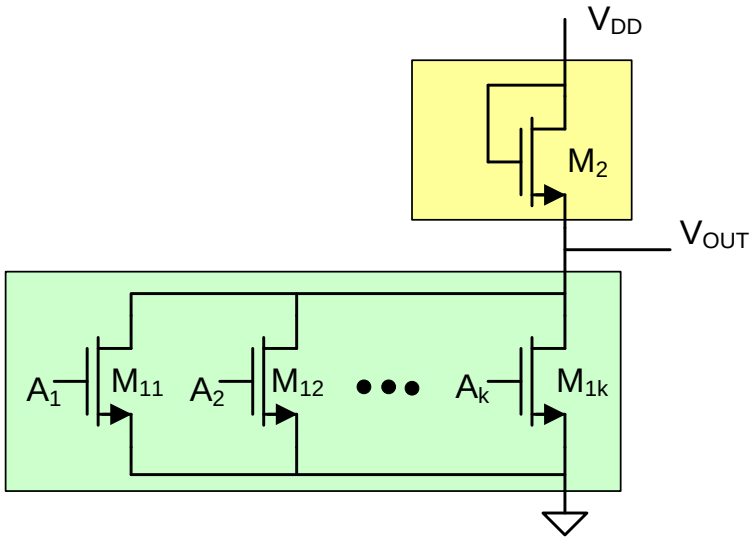


- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when V_{OUT} is low
- Very economical process
- Termed “ratio logic”
- Compact layout (no wells !)

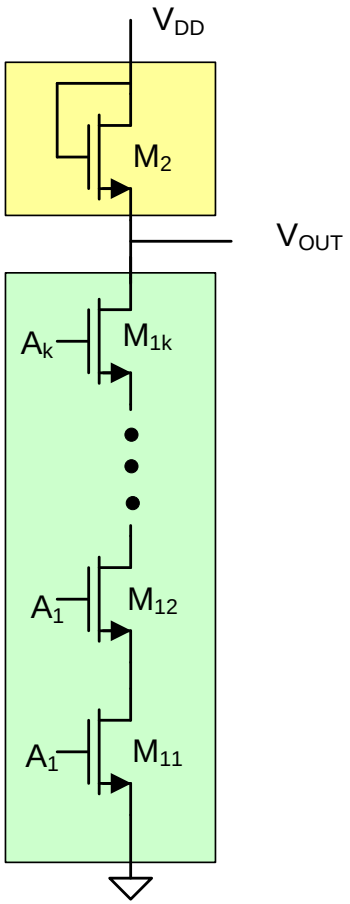
Other CMOS Logic Families



Enhancement Load NMOS



k-input NOR

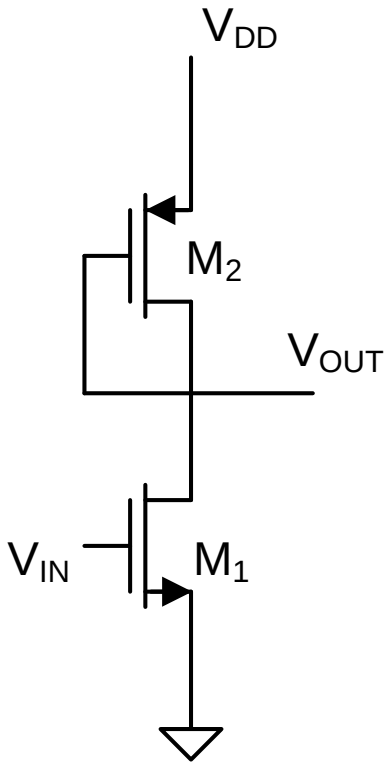


k-input NAND

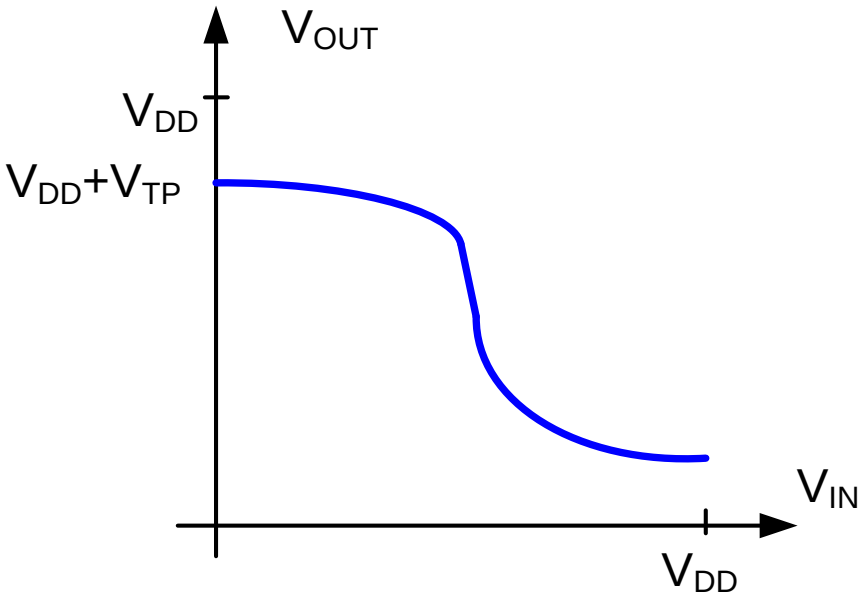
- **Multiple-input gates require single transistor for each additional input**

- **Still useful if many inputs are required (static power does not increase with k**

Other CMOS Logic Families

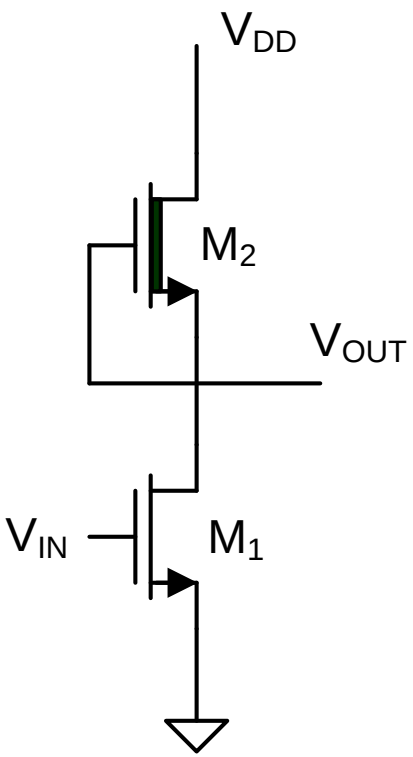


Enhancement Load
Pseudo-NMOS

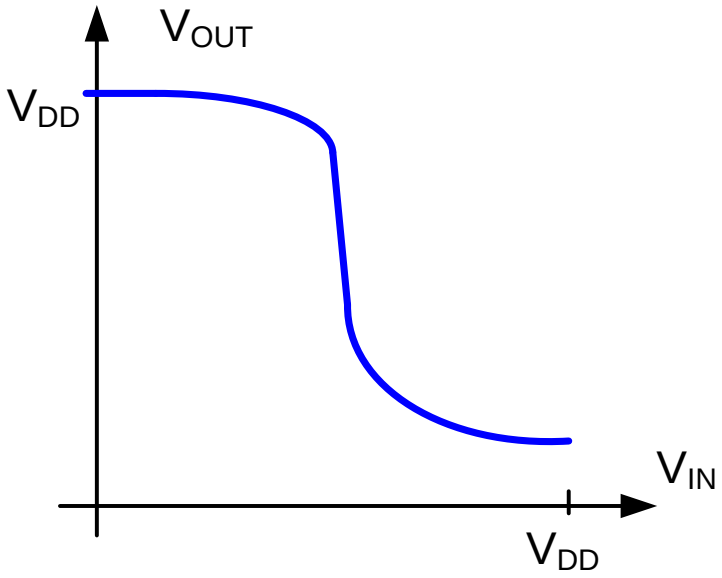


- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when V_{OUT} is low
- Termed “ratio” logic

Other CMOS Logic Families



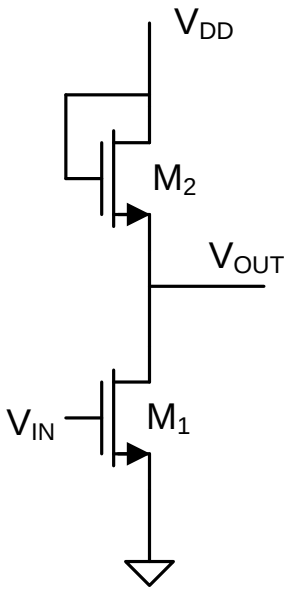
Depletion
Load NMOS



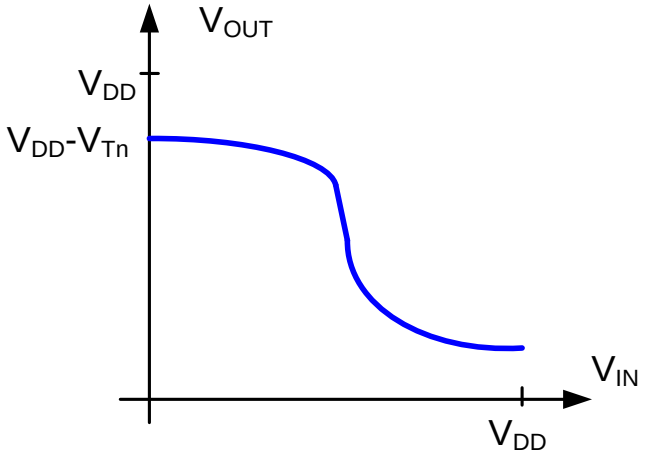
$V_{TD}<0$

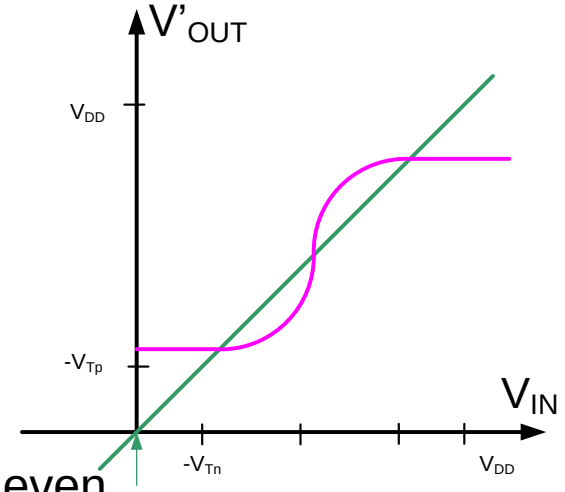
- Low swing is reduced
- Static Power Dissipation Large when V_{OUT} is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells !)
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today

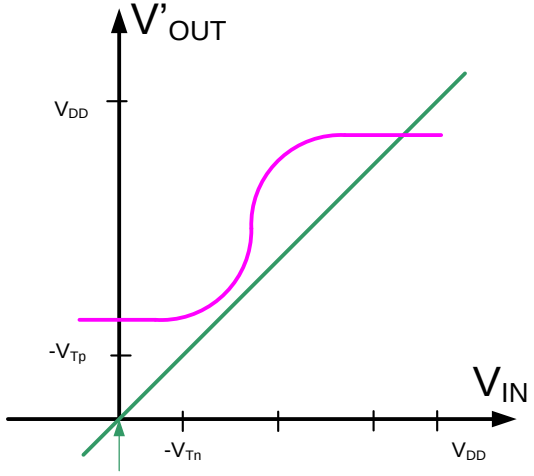
Other CMOS Logic Families



Enhancement
Load NMOS

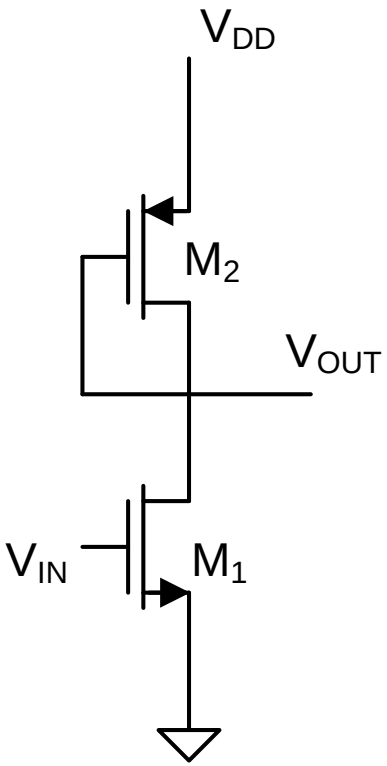




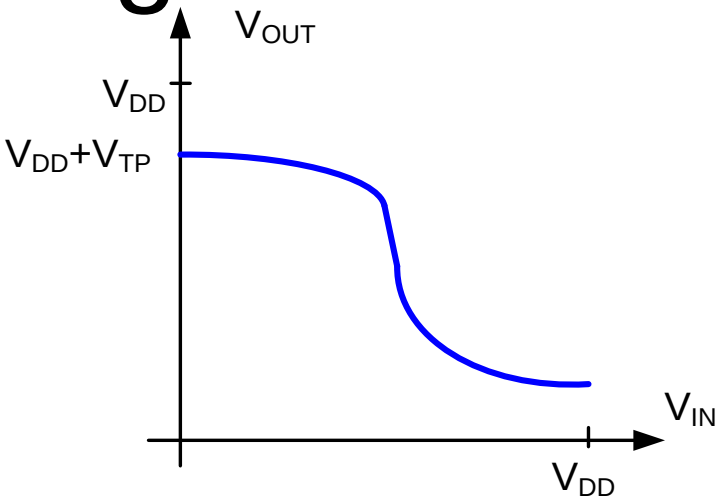


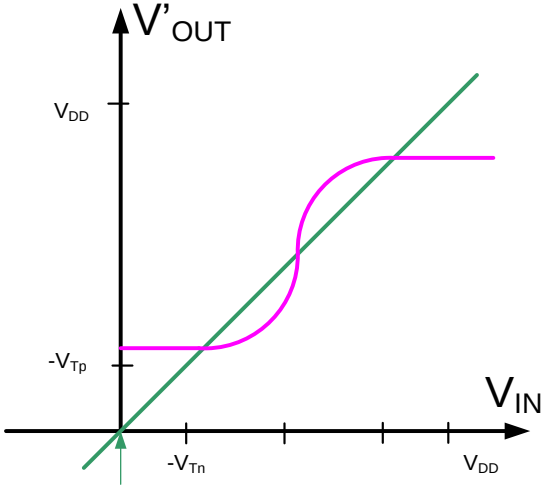
- Reduced V_H-V_L
- Device sizing critical for even basic operation
- Shallow slope at V_{TRIP}

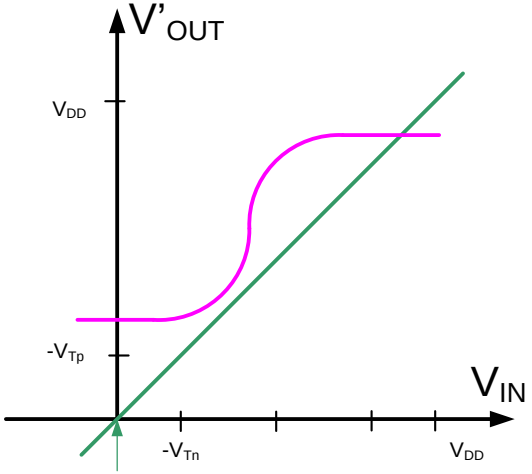
Other CMOS Logic Families



Enhancement Load
Pseudo-NMOS

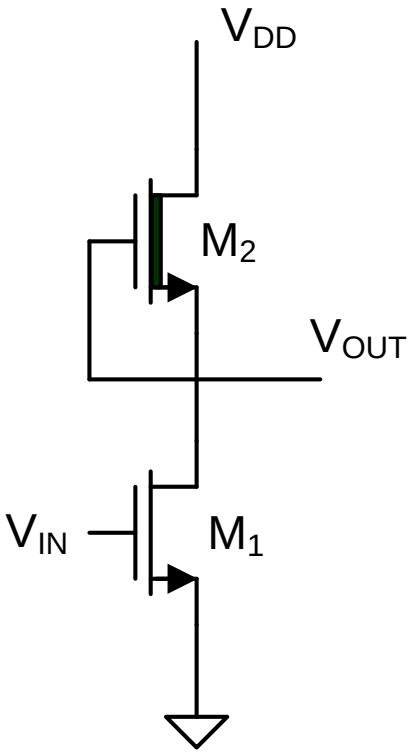






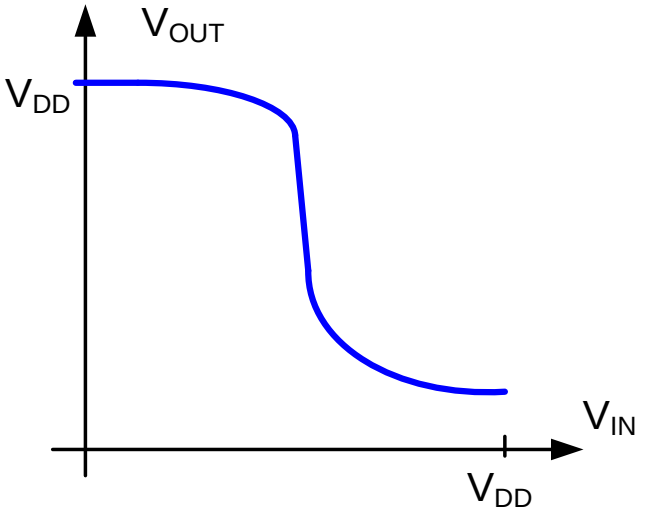
- Reduced V_H-V_L
- Device sizing critical for even basic operation
- Shallow slope at V_{TRIP}

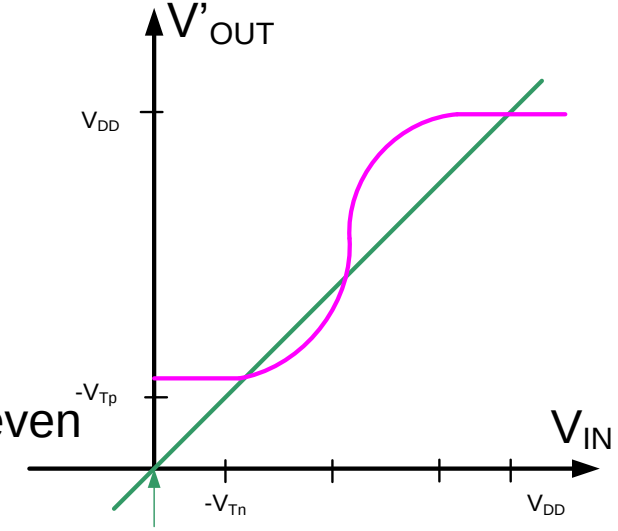
Other CMOS Logic Families

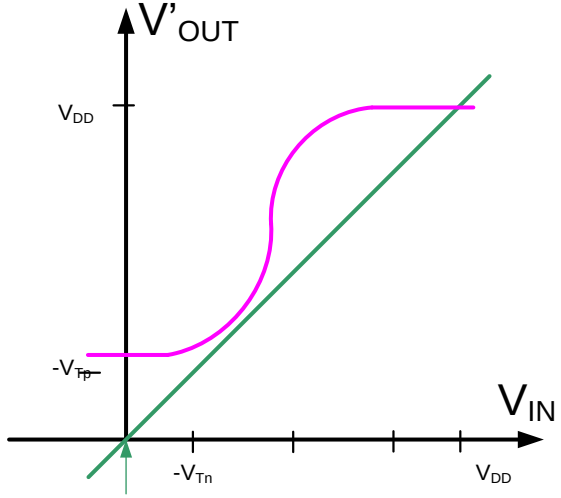


Depletion
Load NMOS

$V_{TD}<0$

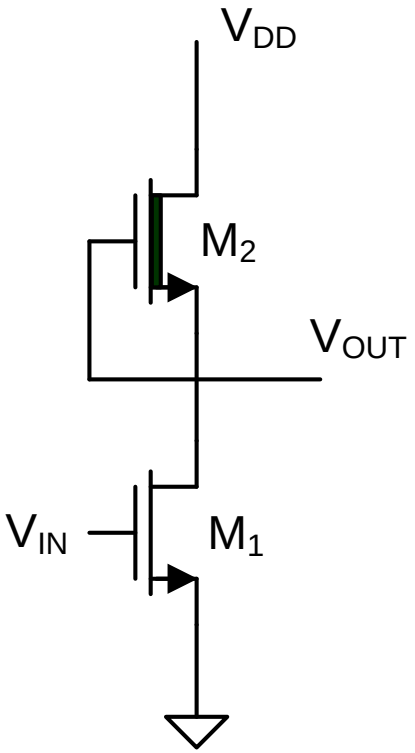






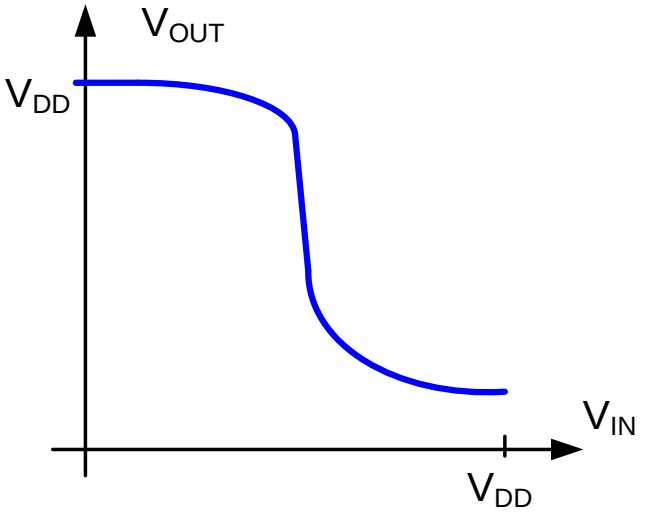
- Reduced V_H-V_L
- Device sizing critical for even basic operation
- Shallow slope at V_{TRIP}

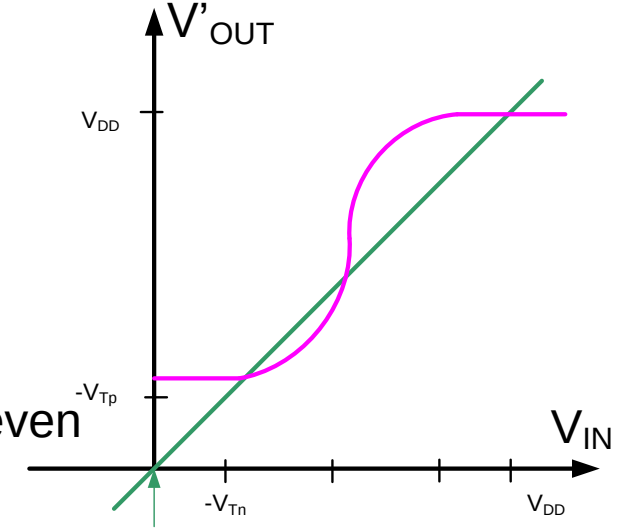
Other CMOS Logic Families

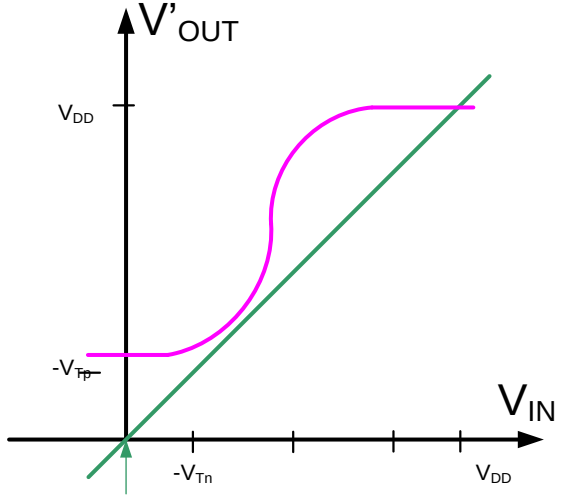


Depletion
Load NMOS

$V_{TD}<0$

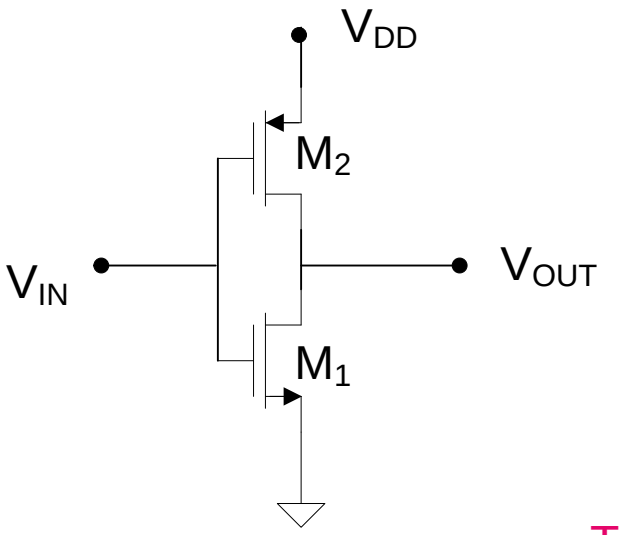






- Reduced V_H-V_L
- Device sizing critical for even basic operation
- Shallow slope at V_{TRIP}

Static Power Dissipation in Static CMOS Family



When V_{OUT} is Low, $I_{D1}=0$

When V_{OUT} is High, $I_{D2}=0$

Thus, $P_{STATIC}=0$

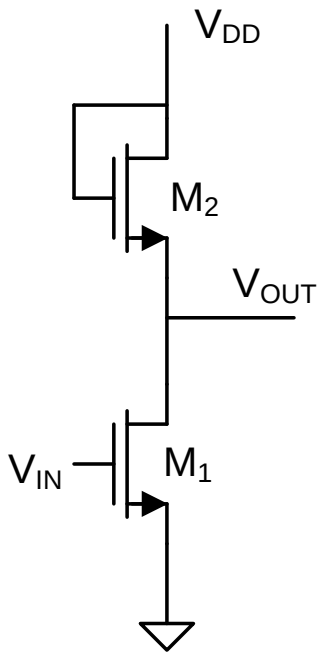
This is a key property of the static CMOS Logic Family and is the major reason Static CMOS Logic is so dominant

It can be shown that this zero static power dissipation property can be preserved if the PUN is comprised of n-channel devices, the PDN is comprised of n-channel devices and they are never both driven into the conducting states at the same time

Static Power Dissipation in Ratio Logic Families

Example:

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L=V_{Tn}



Enhancement Load NMOS

Observe:

V_H=V_{DD}-V_{Tn}

If V_{IN}=V_H, V_{OUT}=V_L so

$$I_{D1} = \frac{\mu C_{OX} W_1}{L_1}\left(V_{GS1} - V_T - \frac{V_{DS1}}{2}\right)V_{DS1}$$

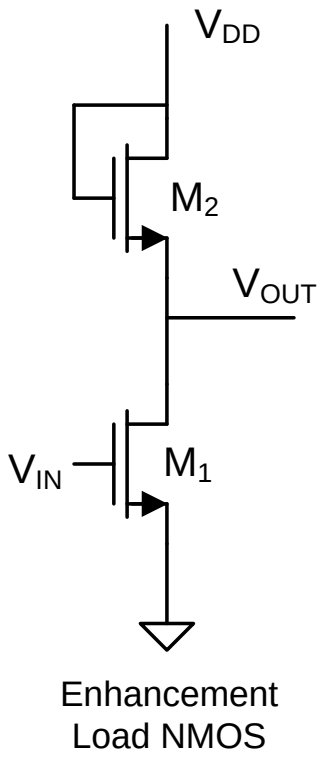
$$I_{D1} = 10^{-4}\left(5 - 1 - 1 - \frac{1}{2}\right)\bullet 1 = 0.25mA$$

P_L=(5V)(0.25mA)=1.25mW

Static Power Dissipation in Ratio Logic Families

Example:

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L=V_{Tn}



Enhancement Load NMOS

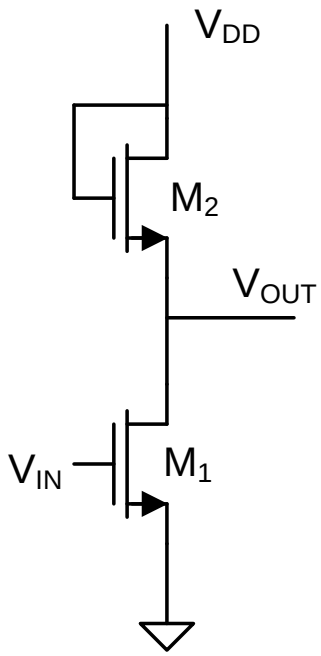
P_L=(5V)(0.25mA)=1.25mW

If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

Static Power Dissipation in Ratio Logic Families

Example:

Assume V_{DD}=5V
V_T=1V, μC_{OX} =10^{-4}A/V^2, W_1/L_1=1 and M_2 sized so that V_L=V_{Tn}



Enhancement Load NMOS

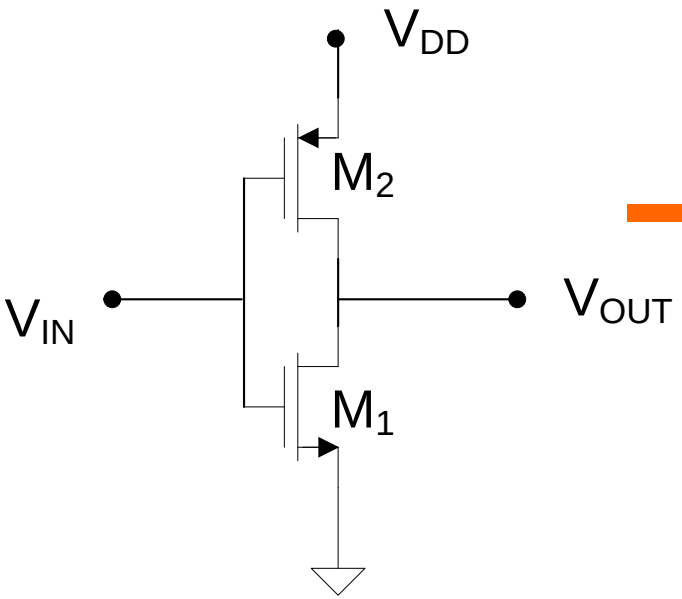
P_L=(5V)(0.25mA)=1.25mW

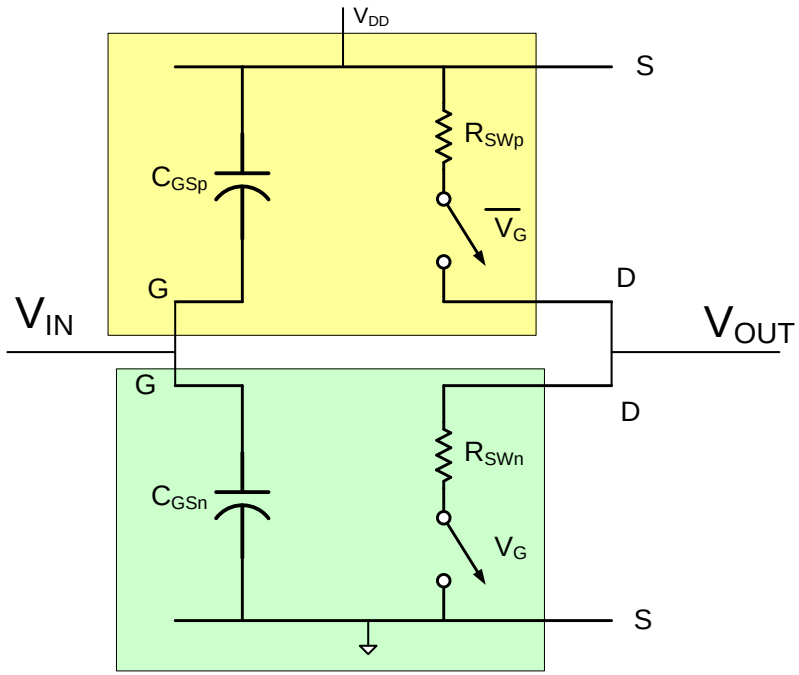
If a circuit has 100,000 gates and half of them are in the V_{OUT}=V_L state, the static power dissipation will be

$$P_{STATIC} = \frac{1}{2}10^5 \bullet 1.25\,mW = \mathbf{62.5W}$$

This power dissipation is way too high and would be even larger in circuits with 100 million or more gates – the level of integration common in SoC circuits today

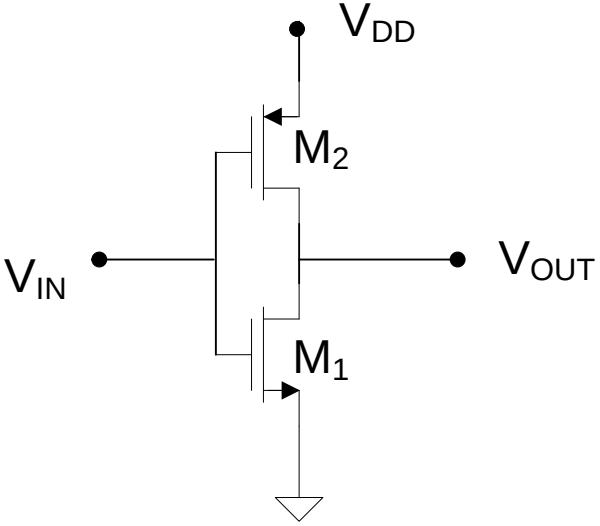
Propagation Delay in Static CMOS Family

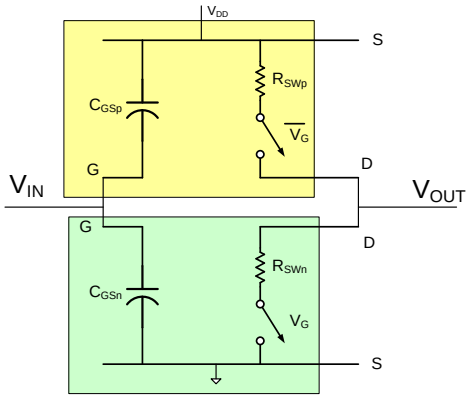


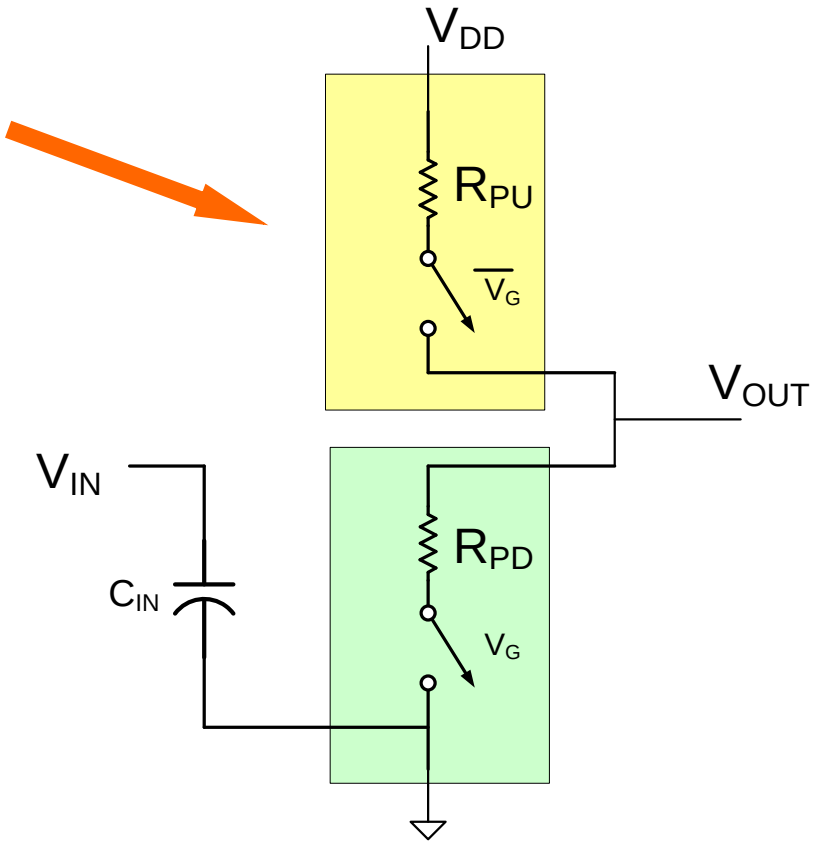


Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family

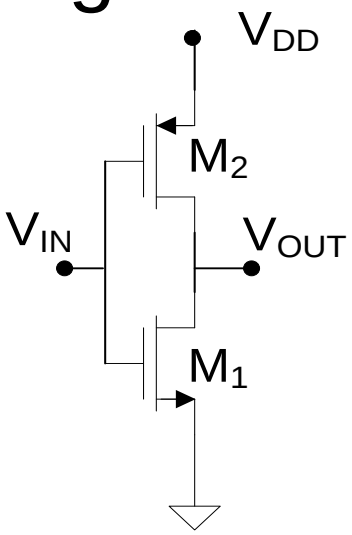


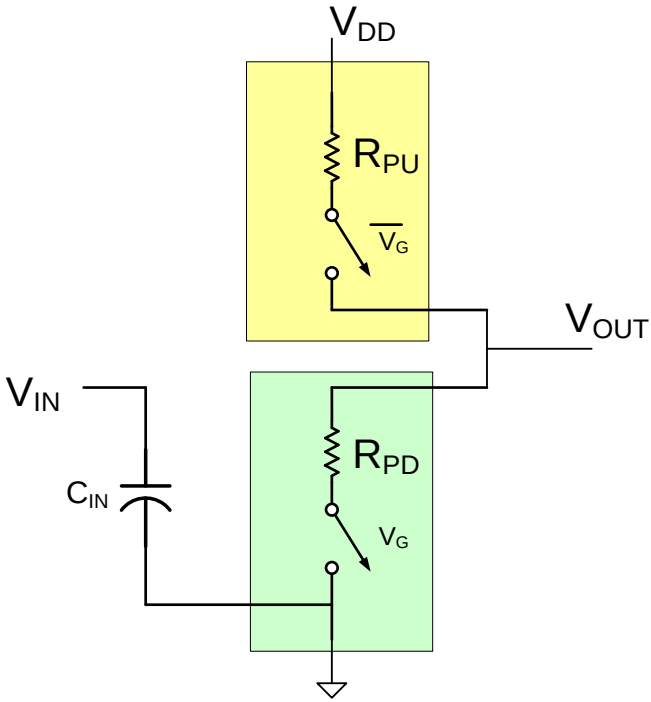




Switch-level model of Static CMOS inverter (neglecting diffusion parasitics)

Propagation Delay in Static CMOS Family





Since operating in triode through most of transition:

$$I_D \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T\right)V_{DS}$$

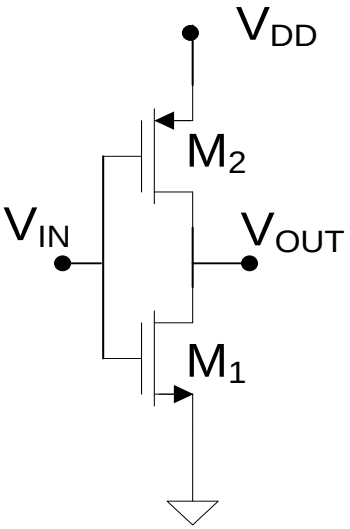
$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 \left(V_{DD} - V_{Tn}\right)}$$

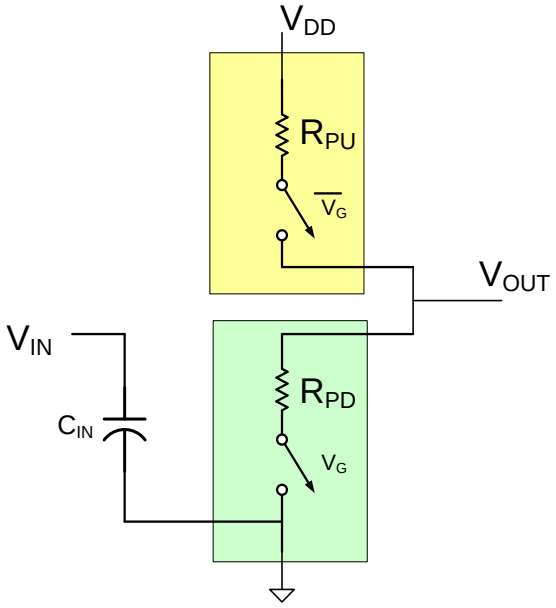
$$I_D = \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \cong \frac{\mu C_{OX} W}{L}\left(V_{GS} - V_T\right)V_{DS}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 \left(V_{DD} + V_{Tp}\right)}$$

$$C_{IN} = C_{OX}\left(W_1 L_1 + W_2 L_2\right)$$

Propagation Delay in Static CMOS Family





$$R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})}$$

$$R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{Tp})}$$

$$C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2)$$

Example: Minimum-sized M_1 and M_2

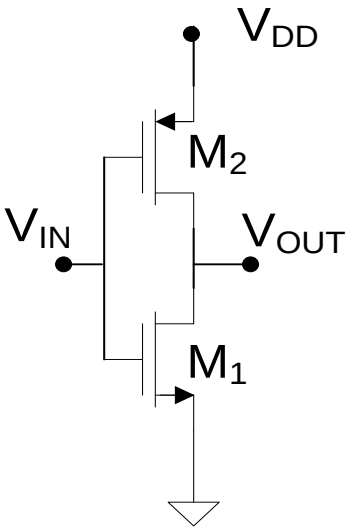
If $u_n C_{OX}=100\mu AV^{-2}$, $C_{OX}=4\ fF\mu^{-2}$, $V_{Tn}=V_{DD}/5$, $V_{TP}=-V_{DD}/5$, $\mu_n/\mu_p=3$, $L_1=W_1=L_{MIN}$, $L_2=W_2=L_{MIN,}$ $L_{MIN}=0.5\mu$ and $V_{DD}=5V$

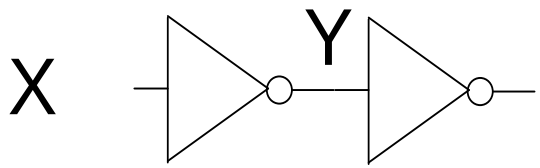
$$R_{PD} = \frac{1}{10^{-4} \bullet 0.8V_{DD}} = 2.5K\ \Omega$$

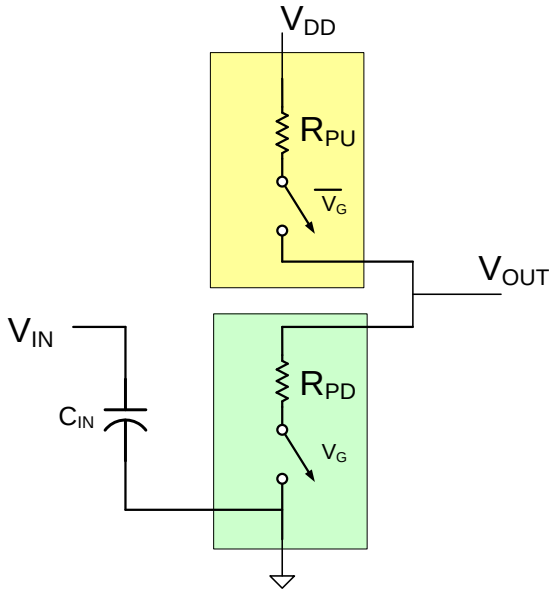
$$C_{IN} = 4 \bullet 10^{-15} \bullet 2L^2_{MIN} = 2fF$$

$$R_{PU} = \frac{1}{10^{-4} \bullet \frac{1}{3} \bullet 0.8V_{DD}} = 7.5K\ \Omega$$

Propagation Delay in Static CMOS Family







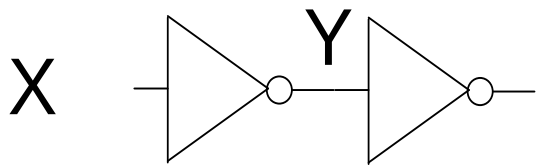
In typical process with Minimum-sized M_1 and M_2 :

$$R_{PD} \simeq 2.5K\Omega$$

$$R_{PU} \simeq 3R_{PD} = 7.5K\Omega$$

$$C_{IN} \simeq 2fF$$

Propagation Delay in Static CMOS Family

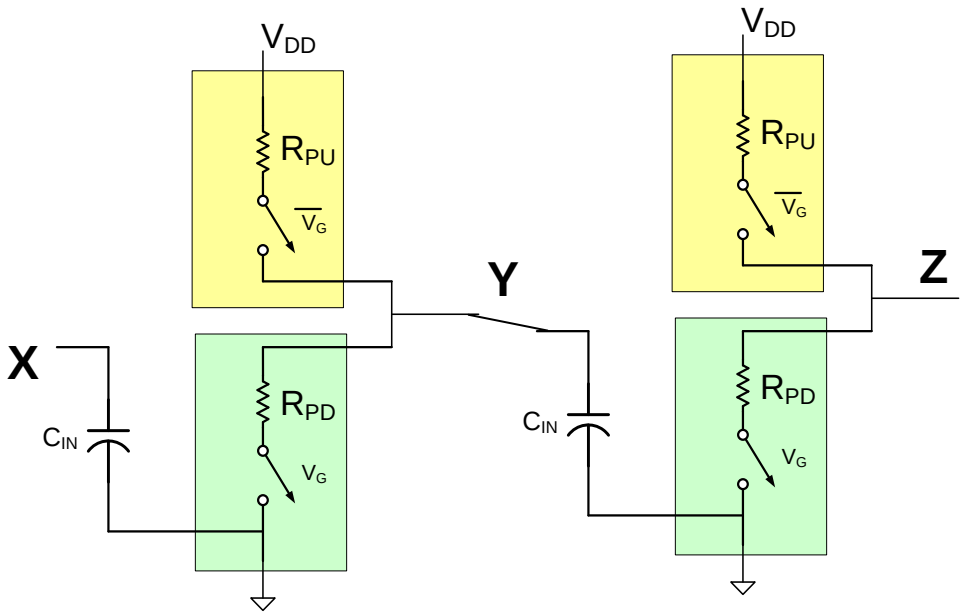


In typical process with Minimum-sized M_1 and M_2 :

$R_{PD} \simeq 2.5K\Omega$

$R_{PU} \simeq 3R_{PD} = 7.5K\Omega$

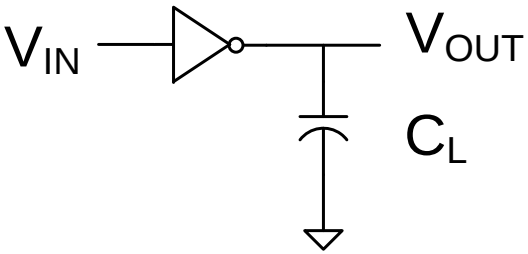
$C_{IN} \simeq 2fF$



How long does it take for a signal to propagate from x to z?

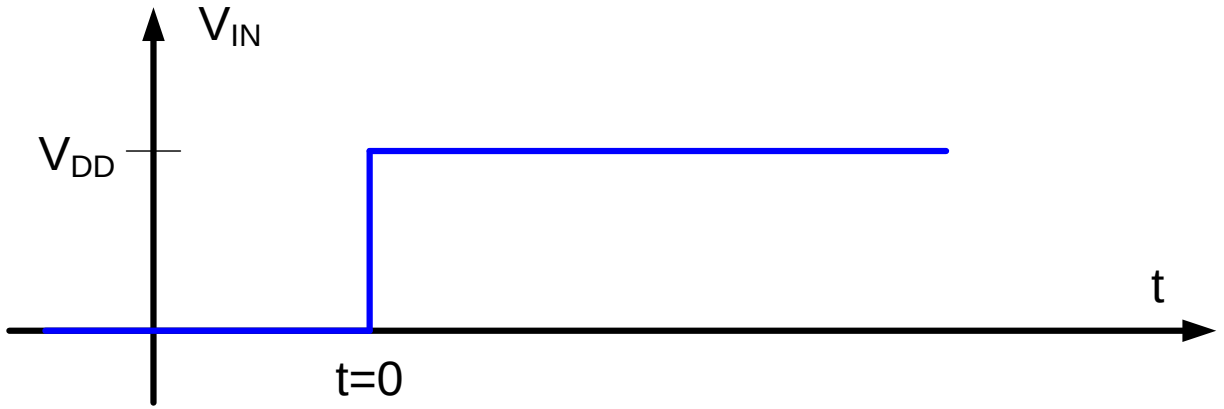
Propagation Delay in Static CMOS Family

Consider:



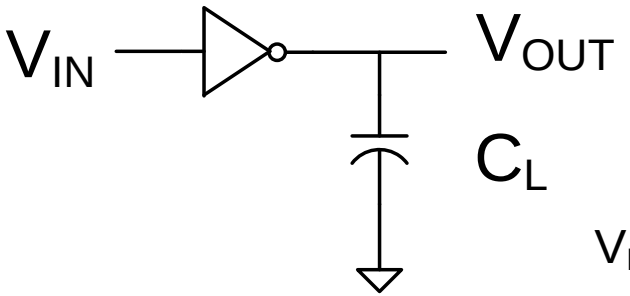
For HL output transition, C_L charged to V_{DD}

Ideally:

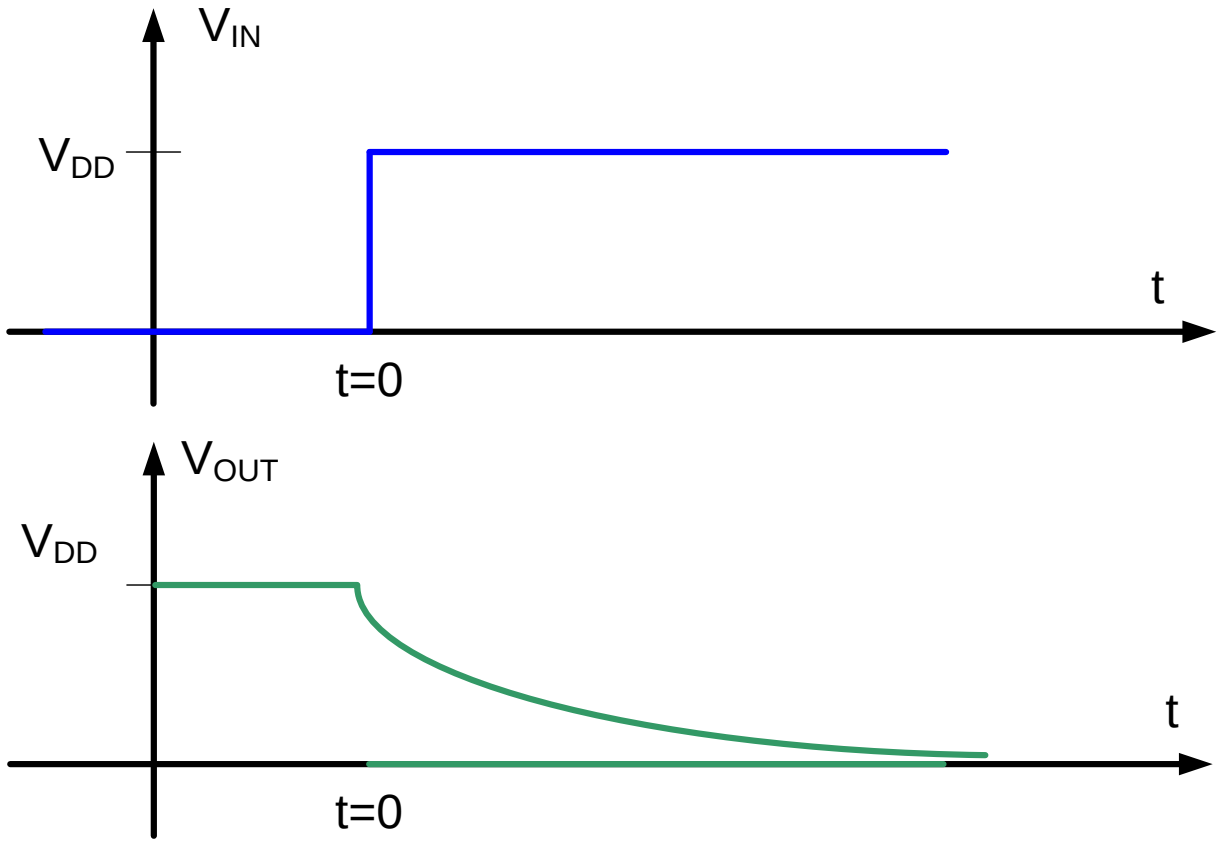


Propagation Delay in Static CMOS Family

For HL output transition, C_L charged to V_{DD}

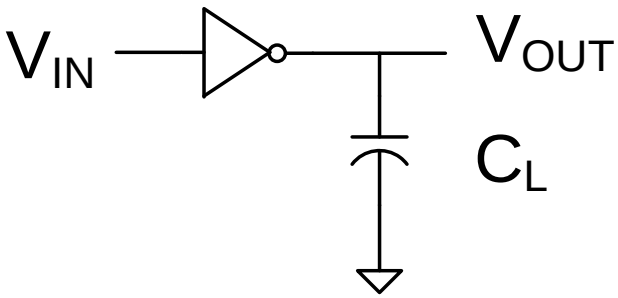


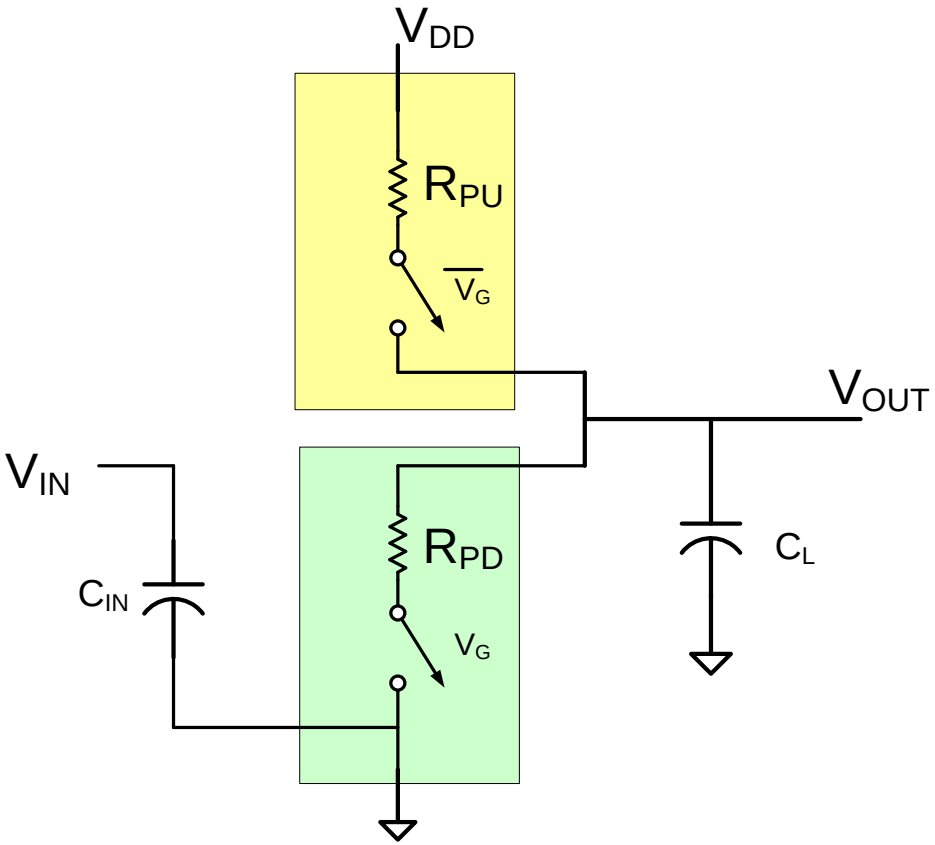
Actually:



What is the transition time t_{HL} ?

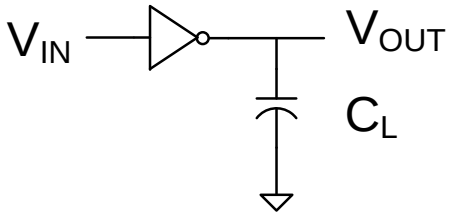
Propagation Delay in Static CMOS Family

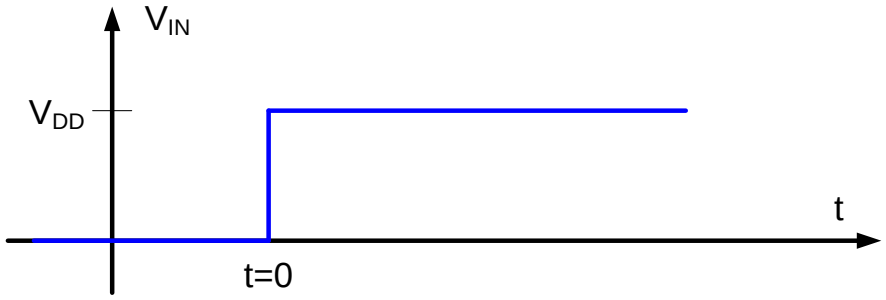


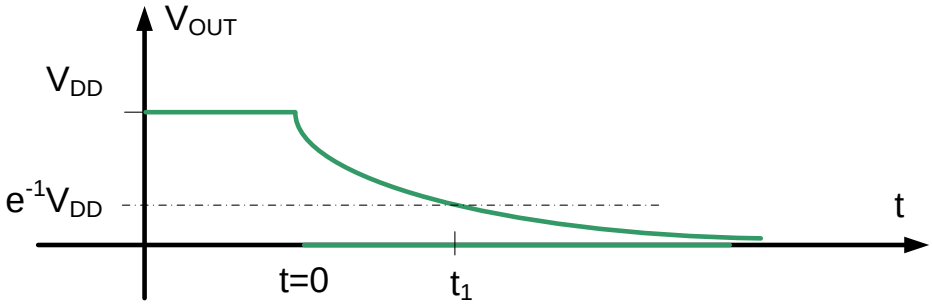


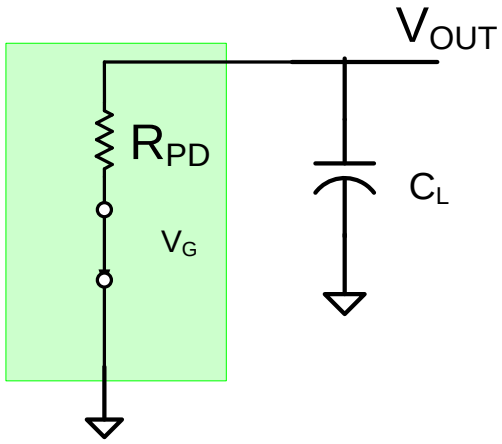
Propagation Delay in Static CMOS Family

For HL output transition, C_L charged to V_{DD}









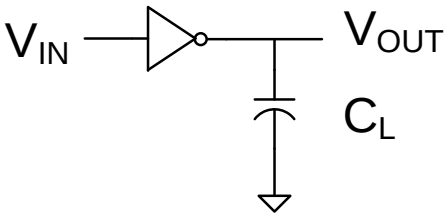
$$V_{OUT}(t) = F + (I - F)e^{\frac{-t}{\tau}} = 0 + (V_{DD} - 0)e^{-\frac{t}{R_{PD}C_L}}$$

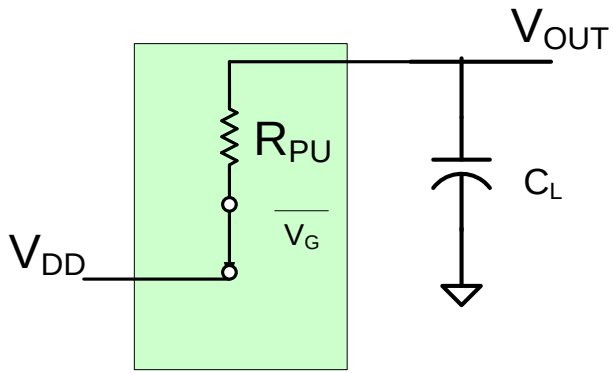
$$\frac{V_{DD}}{e} = V_{DD}\, e^{-\frac{t_1}{R_{PD}C_L}} \quad \Rightarrow \quad t_1 = R_{PD}C_L$$

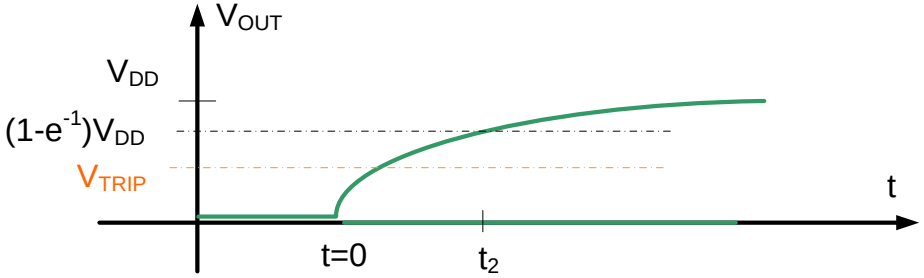
If V_{TRIP} is close to $V_{DD}/2$, t_{HL} is close to t_1

Propagation Delay in Static CMOS Family

For HL output transition, C_L charged to V_{DD}







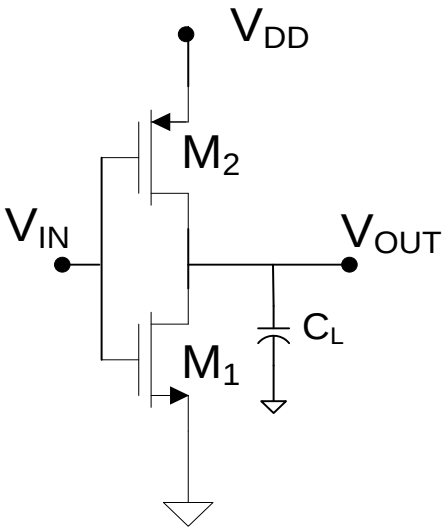
$$t_{LH} \cong t_2 = R_{PU} C_L$$

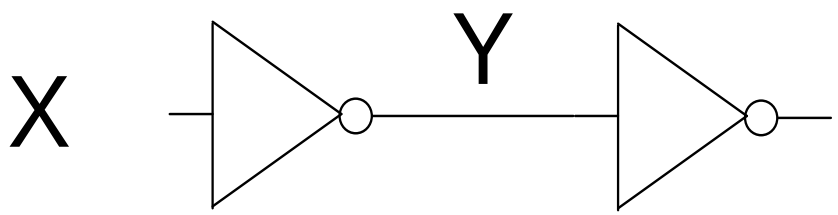
Summary:

$$t_{LH} \cong R_{PU} C_L$$

$$t_{HL} \cong R_{PD} C_L$$

Propagation Delay in Static CMOS Family





In typical process with Minimum-sized M_1 and M_2 :

$$t_{HL} \cong R_{PD}C_L \cong 2.5K \bullet 2fF = 5ps$$

$$t_{LH} \cong R_{PU}C_L \cong 7.5K \bullet 2fF = 15ps$$

Note: LH transition is much slower than HL transition

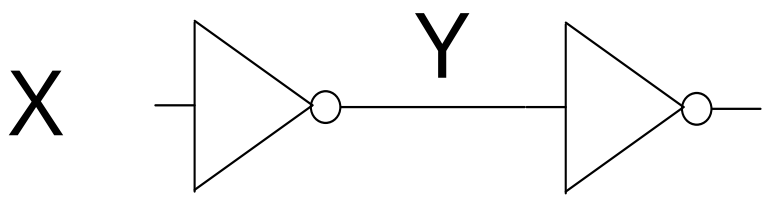
Propagation Delay in Static CMOS Family

Defn: The Propagation Delay of a gate is defined to be the sum of t_{HL} and t_{LH}, that is, $t_{PROP}=t_{HL}+t_{LH}$

$$t_{PROP} = t_{HL} + t_{LH} \cong C_L \left(R_{PU} + R_{PD} \right)$$

Propagation delay represents a fundamental limit on the speed a gate can be clocked

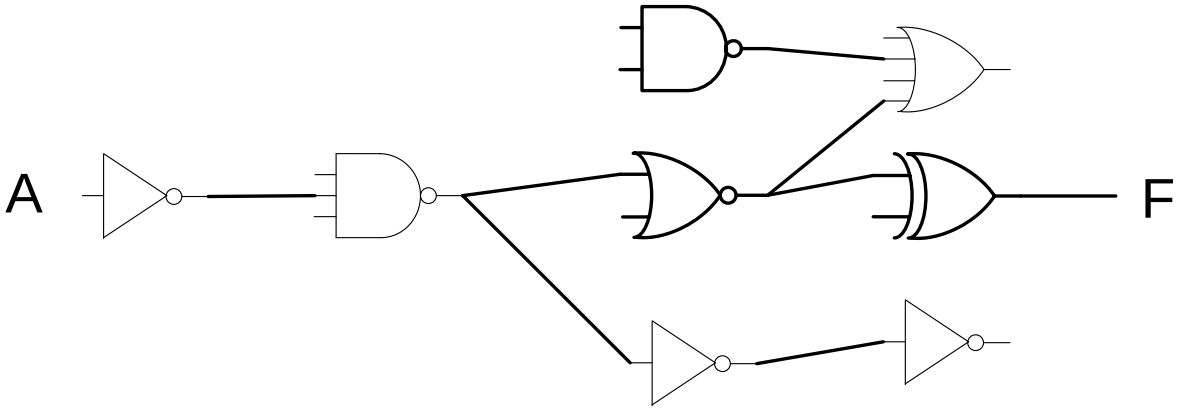
For basic two-inverter cascade in static CMOS logic



In typical process with minimum-sized M_1 and M_2 :

$$t_{PROP} = t_{HL} + t_{LH} \cong 20\,p\,\text{sec}$$

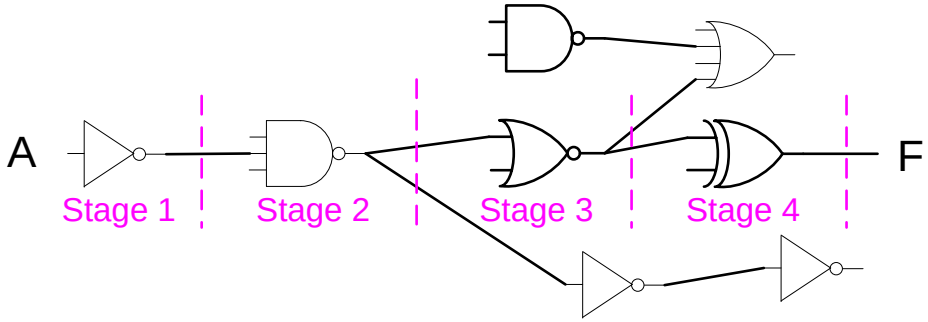
Propagation Delay in Static CMOS Family



The propagation delay through k levels of logic is approximately the sum of the individual delays in the same path

Propagation Delay in Static CMOS Family

Example:



$$t_{HL}=t_{HL4}+t_{LH3}+t_{HL2}+t_{LH1}$$

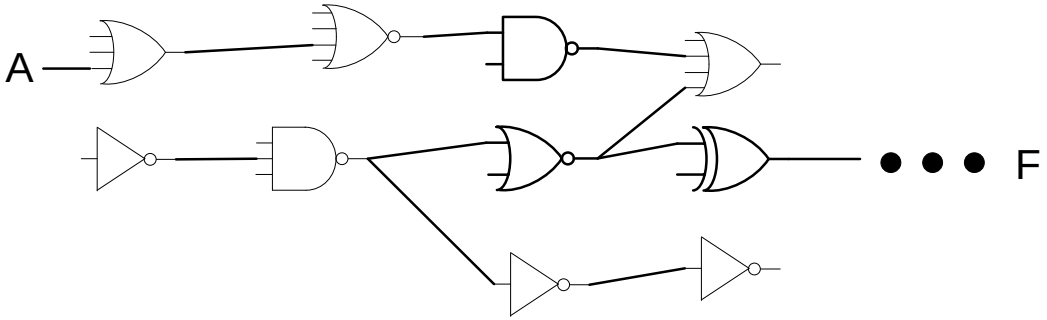
$$t_{LH}=t_{LH4}+t_{HL3}+t_{LH2}+t_{HL1}$$

$$t_{PROP}=t_{LH}+t_{HL}=(t_{LH4}+t_{HL3}+t_{LH2}+t_{HL1})+(t_{HL4}+t_{LH3}+t_{HL2}+t_{LH1})$$

$$t_{PROP}=t_{LH}+t_{HL}=(t_{LH4}+t_{HL4})+(t_{LH3}+t_{HL3})+(t_{LH2}+t_{HL2})+(t_{LH1}+t_{HL1})$$

$$t_{PROP}=t_{PROP4}+t_{PROP3}+t_{PROP2}+t_{PROP1}$$

Propagation Delay in Static CMOS Family



Propagation through k levels of logic

$$t_{HL} \simeq t_{HLk} + t_{LH(k-1)} + t_{HL\,k-2} + \bullet\bullet\bullet + t_{XY1}$$

$$t_{LH} \simeq t_{LHk} + t_{HL(k-1)} + t_{LH\,k-2} + \bullet\bullet\bullet + t_{YX1}$$

where x=H and Y=L if k odd and X=L and Y=h if k even

$$t_{PROP} = \sum_{i=1}^{k} t_{PROPk}$$

End of Lecture 37